Keynote: Design Challenges for advanced CMOS

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Abstract

GLOBALFOUNDRIES is committed to develop and deliver a high level of design enablement to our customers. As part of this strategy GLOBALFOUNDRIES has developed a series of digital design structures which are enabled in parallel to the technology development. These digital design structures allow the concurrent development and optimization of design rules, process development kits, EDA implementation tools and physical IP as standard cells and memory macros. This presentation will outline the specific test structures and their application to the digital design enablement in 28nm, 20nm, and 14nm advanced technologies. One digital design structure resembles a system-on-chip design based on an ARM Cortex series dual-core CPU.

Curriculum Vitae

Dr. Joerg Winkler is a Fellow Design Engineer at GLOBALFOUNDRIES. In this role, he is focused on digital design developments and design / technology co-optimization for leading edge technology nodes.

Dr. Winkler has worked in semiconductor digital design for the past 19 years, most of that time with AMD and GLOBALFOUNDRIES. With AMD he was chip architect in the areas of communications, x86 chipsets, and northbridge for AMD's x86 Fusion APU's. He began his career with the Fraunhofer Institute of Microelectronic Systems in Dresden, Germany.

Dr. Winkler holds graduate and doctoral degrees from Dresden Technical University.