

## 3D Integration for Multimedia Applications

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### Abstract:

Multimedia applications are facing new challenges with embedded networking features and 3D needs, graphic and vision. These features are creating challenges in term of systems, architecture split, signal integrity, power dissipation and thermal effects. Interconnect limits, reached with wire bonding, are opening new areas with conceptual changes pushing the 3D integration adoption in a “More Than Moore” way. The 3D integration should be strongly linked with efficient cost analysis and with new EDA solutions.

Interconnect delays with good signal integrity are pushing major design changes: high bandwidth memory interfaces, architectural CPU/bus/caches split and mixed integration with different domains. DDR interfaces in multimedia are sooner breaking the 1Gbps barrier with very low clock jitter. The “More Moore” CMOS scaling copes with larger integration for System on Chip (SoC), nevertheless inter die RC delay cannot follow the move. Beyond flip-chip solder bump, the move to finer pitch bumps is pushing the product integration with the substrate/package/board constraints inside SoC architecture.

A new EDA solution system with higher level language and modelling is required. The bulk of the solution should be an user centric approach taking the benefit of previous experience. The basic approach is to have an early accurate cost evaluation of systems enabling the architecture split, which then gives an accurate schedule on developments made concurrently.

A multimedia product has to cope with very dynamic markets. Multimedia products are taking the benefit of validated HW and SW solutions to address new needs with new concepts. Right cost at the right time is a key for multimedia applications.

### Curriculum Vitae:



Dominique Henoff is director of Advanced Technology and Innovation in Home Entertainment Group at STMicroelectronics. His responsibilities include process choice, design solutions, SoC architecture development and associated EDA tools. He started his career in MATRA then BULL on microprocessor systems and VLSI design. In 1994, he joined STMicroelectronics on the 64bit microprocessor development then move in 1999 in US, as program manager, for the SH5 with Hitachi. Back to Europe in 2002, he developed design solutions for nanotechnologies then managed MPEG4 SoC designs.

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