Synergies to Enable a Designer-Driven Assertion-Based Verification Methodology

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Abstract

The last few years have dramatically improved technologies like functional coverage, formal verification, semi-formal methods and assertion-based verification. While the emergence of break-through EDA tools is crucial to keep pace with design complexities, the real challenge for large industrial projects is the successful deployment of these technologies into an evolving design and verification methodology. Design teams are tired of trying out new buzzword technology every year, especially if these just add new workload on top of existing tasks.

The verification methodology for IBM microprocessor and systems development (PowerPC, Cell, G5, p-Series, z-Series) has to scale from functional units to chips containing large systems. A critical part of maintaining a leading-edge verification flow is the ability to systematically improve and adapt it without breaking successful existing technology and practices.The latest evolutionary step for the IBM verification methodology was to embrace the assertion-based verification driven by designers. This extension will be used as a case study to demonstrate principles of how to drive positive technology change into an existing, successful design and verification community.

Curriculum Vitae

Wolfgang Roesner got his PhD in electrical engineering at the University of Kaiserslautern, Germany, before he joined the IBM development lab in Böblingen in 1984. There he developed simulators and hardware design languages, later joining the POWER processor development team, where he co-developed the Texsim cycle-based simulation system. His verification tools have been used on all IBM CMOS microprocessor projects, and since 1996 he has been responsible for the overall strategy of verification tools development. Since 2003 he is responsible for IBM Systems Group's verification methodology and is server verification lead.