Multi-Mode Power Reduction for Mobile Application Chips

edaForum05 Presentation

Technical Session I

Knut Just

Infineon Multi-Mode Power Reduction for Mobile Application Chips

Abstract

Today s devices for mobile applications, such as GSM/EDGE/ UMTS baseband chips, demand high processing performance in terms of processor speed and low power dissipation. However, the performance demands vary strongly, depending on phone modes and activities e.g. stand-by mode vs. talk mode vs. high performance application modes such as video processing and gaming.

In recent years several low power features have been developed to address both the static leakage power consumption and the dynamic active power consumption. These features, or a combination of them, can be tailored to dynamically varying performance needs of the chip in different modes meaning different use cases.

The first challenge of now and the future is to optimize the timing, power and area for different modes simultaneously with the EDA tools for RTL logic synthesis, timing driven layout, and static timing analysis. The second challenge is to verify the correct implementation of all low power features in simulation, structural netlist checks, and at the production tester.

Biography

Knut Just Principal, Digital Design Methodology Infineon Technologies AG, Germany

He received his PhD in electrical engineering from the Technical University of Munich, Germany, before he joined Siemens Semiconductors (now Infineon Technologies) in 1987. He was with the CAD department until 1995, being responsible for FE-Tools for logic synthesis und test. As project manager for development of chips for GSM baseband, GPS, und WLAN he joined the Wireless Solutions Business Group. From 2001 until 2003 he was project manager for the Infineon Low Power/Low Voltage project for the 90 nm technology node where the team developed low power features in the fields of technology, cell libraries memories, and design architectures. In the Digital Design Methodology Group since 2002, he is responsible for low power methodologies and the interface between chip project needs and the library and

memory development.

edacentrum | Schneiderberg 32 | 30167 Hannover | fon: +49 511 762-19699 | fax:+49 511 762-19695 | email: info edacentrum [dot] denach oben

---