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# EDA Tools and Methodologies: A Synopsys Perspective

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## Abstract

Historically, designers have been able to create their designs and intellectual property without worrying too much about what manufacturers would do once the designs were handed off to them, or what systems companies would do with the final chips. Designers' jobs were already so complex that they could not spend time on seemingly tangential concerns.

Then the picture changed. Yield issues that arose at 130 nm surprised everyone along the IC value chain, resulting in a new look at who needs to be concerned with what. The days of independent system design, mixed signal chip design, IP integration, and manufacturing are over. Chip design can and will increasingly impact power, yield, and cost of manufacturing; and process technologies will increasingly impact design methodology. Likewise, both chip design and manufacturing will impact which systems get to market, and the ability of such systems to target large volume applications.

This new picture, exacerbated by the move to 90 and 65 nm, is driving the need for complete and correlated EDA platforms aimed at concurrently addressing such inter-related challenges and making the process less painful for all concerned. The day of relentless demand for global technology partnerships and support has arrived.

To that end, Synopsys provides system-level to silicon-level verification, a complete front-to-back design and test environment, design reuse technology, and global professional services to help its customers get their silicon working quickly and accurately. Synopsys solutions include pre-designed and compliant analog and digital blocks of IP that can be easily inserted into design flows, as well as technology to address yield and manufacturing issues early in the design process.

In this presentation, Synopsys addresses these challenges and future possibilities facing designers, and discusses the tools and methodologies with which Synopsys is responding.

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