Talk 1: Towards Trustworthy RISC-V Processors for Safety-critical Applications

Eyck Jentzsch, MINRES Technolgies GmbH, DE

Abstract

RISC-V is one of the hottest trends in the industry these days, with its mature software toolchain and many hardware processor providers offering implementations ranging from textbook open-source cores to high-end commercial ones. The freedom to configure and customize the RISC-V ISA in accordance to the system needs, including custom instructions, is one of its strongest appeals, making custom RISC-V CPUs an attractive choice for an unprecedented number of companies. However, the challenge of actually designing a RISC-V core with custom extensions and ensuring its correct functional behaviour is still significant, even more in environments with high safety and security expectations. In this session, we present an automated flow to generate RISC-V cores with custom extensions together with their complete verification.

Biography

 Eyck Jentzsch holds a Dipl-Ing. from the Technical University Ilmenau and has more than 25 years experience in microelectronics and semiconductor design. He is working at MINRES as General Manager and focuses on virtual platform modelling, development, and application as well as RISC-V IP development and verification. Prior to that he worked at Cadence Design Systems Inc. and Siemens in various full- and semi-custom as well as system level design and verification positions.