



Veröffentlicht auf *edacentrum* (<https://www.edacentrum.de>)

[Startseite](#) > Druckeroptimiertes PDF

Invited Talks

Invited Talks at REES 2017

Title: Design-for-Resiliency in Dynamically Power Managed Systems

Speaker: Liangzhen Lai, ARM Ltd.

Abstract: Almost all reliability-related phenomena have strong dependence on the circuit operating conditions, e.g., voltage/temperature, which are typically determined or controlled by dynamic power management mechanisms. Whether intentionally or unintentionally, different power reduction mechanisms and corresponding management schemes can impact the hardware reliability and system resiliency in one way or the other. In this talk, we first examine the resiliency issues related to dynamically power-managed systems. Then we demonstrate how reliability issues can be mitigated by different implementation of the power management mechanisms all the way from circuit to system software. We will also demonstrate how resiliency can be achieved by utilizing different alternative power management mechanisms without sacrificing performance and power savings.

Title: Multi-Layer-Resilience: The need for Discipline

Speaker: Prof. Dr. Wolfgang Ecker, Infineon Technology

Authors: Bogdan Tabacaru, Moomen Chaari, Wolfgang Ecker, Infineon Technology

Abstract: Safety analysis requires a lot of simulations to validate robustness of design and to prove that failure rate and failure detection rate is below a given threshold. These simulations are executed at gate level. They run realistic stimuli with many threads modeled by stuck-at-faults. Performing these simulations at higher levels is one measure to cope with the complexity of all these simulations. To avoid wrong faults, a discipline must be followed, which we call matching points.

Title: Error Effect Simulation for Automotive using SystemC Virtual Prototypes

Speaker: Dr. Andreas Mauderer, Robert Bosch GmbH

Abstract: In the automotive domain, advanced driver assistance systems (ADAS) increase comfort, which strongly depend on reliable working electronics. The trend goes clearly towards autonomous driving to relieve humans in traffic. As a consequence to the needed high computing performance for ADAS, the complexity of IC's must increase. At the same time functional safety becomes increasingly important in safety critical electronic systems to improve the reliability especially in critical situations. Safety critical domains are e.g. the automotive domain, which this contribution is focused on, avionics, military, medicine, etc. This leads to an increase of the safety requirements, which have to be satisfied.

Hence, functional safety becomes a challenging requirement for the industry. In order to evaluate safety mechanisms in early design phases, we present an error effect simulation environment. It comprises various error injectors for SystemC signals, TLM connections and pure C++ components to address typical elements in VPs.

Title: Novel ISO26262 Compliant Architecture for Advanced Driver Assistance Systems

Speaker: Luc van Dijk, NXP Semiconductors

Abstract: Functional safety is getting more and more important in automotive systems, driven by Advanced Driver Assistance Systems (ADAS) and the development of autonomous cars, not only will this have an impact on the associated hardware and software, it also requires a dedicated way of working, which will be briefly discussed in the first part of the presentation. After that a detailed view of a novel ISO26262 compliant Architecture for ADAS will be presented.

Current and future developments related to functional safety, like Fault tolerant systems and aging detection systems will be reviewed at the end of the presentation, which also covers discussion of the future revision of the ISO26262 standard.

Title: Simultaneous Measurement of Defect Coverage and Tolerance in AMS ICs for ISO26262

Speaker: Stephen Sunter, Mentor Graphics

Abstract: Published data for mixed-signal IC failures in automotive applications shows that the vast majority of the failures are attributable to the analog portion of the ICs, due to test escapes and insufficient reliability. This presentation will describe an analog defect simulator, built on a widely used mixed-signal simulator, that can simultaneously measure a test suite's coverage of potential manufacturing defects with guard-banded test limits, and the circuit's tolerance to reliability defects with specification limits and built-in monitoring for safety as required by ISO 26262. This allows IC designers to provide an automated and objective assessment of likelihood-weighted defect coverage and defect tolerance, in less time, when these metrics are required by Tier 1 automotive customers.

Back to [REES](#) ^[1] website

edacentrum | Schneiderberg 32 | 30167 Hannover | fon: +49 511 762-19699 | fax:+49 511 762-19695 | emailinfo@
edacentrum [dot] denach oben

Quell-URL: <https://www.edacentrum.de/rees/invited-talks>

Links:

[1] <http://www.edacentrum.de/rees>