Controlling leakage power in nanometer CMOS: Technology meets design

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- [Arrival]
- [Hotels]
- [On-demand Training]
- [About edacentrum]

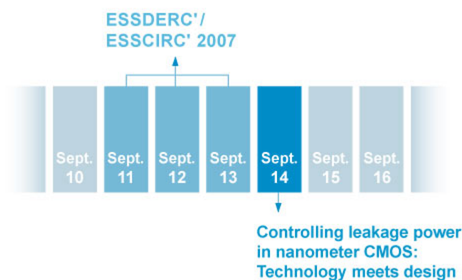
Leakage power is becoming a significant part of the global IC power budget requiring novel circuit design solutions in addition to innovation in technology leakage control techniques. The Workshop will strongly focus on leakage aware design techniques and the technological possibilities to reduce leakage. In addition, the state of the art and future research directions on leakage control from the technology to design techniques at different levels of abstraction will be presented.

Information / Registration

Date and Location:

The workshop will take place on **Friday, September 14, 2007** at Technical University Munich (TUM) in Germany in conjunction with the **35th Solid-State Device Research Conference ESSDERC'2007 and the 31st Solid-State Circuits Conference ESSCIRC'2007**.

TU Munich [1]
Theresienstr. 90
80333 München
Germany



Duration:

One full day

Program:

Time	Title	Speaker
8:30	Registration	edacentrum
9:00	Welcome	Joan Figueras, UPC Barcelona, Spain, CLEAN Training Leader Herman E. Maes, IMEC Leuven, Belgium, PullNANO Training Leader
9:05	Overview of the CLEAN Integrated Project	Roberto Zafalon, ST Microelectronics Italy, CLEAN Coordinator
9:15	Overview of the PullNANO Integrated Project	Dominique Thomas, ST Microelectronics France, PullNANO Board Chairman
9:25	Perspectives on Technological Options to control leakage in advanced Si CMOS devices	Thomas Hoffmann, IMEC, Belgium
9:55	Coffee break	
10:25	High-gate stacks: the solution for leakage reduction?	Luigi Pantisano, IMEC, Belgium
10:55	Leakage Currents in Nanometer CMOS Devices	Thomas Schulz, Infineon, Germany
11:25	Leakage and Leakage Variability in nano-CMOS devices	Asen Asenov, University of Glasgow, United Kingdom Jürgen Lorenz, FhG-IISB, Erlangen, Germany
11:55	Leakage Reduction in sub-100nm CMOS Technologies: Bridging the Gap between Technology, Circuit Design and Product Requirements	Christian Pacha, Infineon, Germany
12:40	Lunch	
14:10	Invited Keynote: High Level Energy and Power Reduction Strategies	Christian Piguet, CSEM, Switzerland
14:55	Circuit Level Leakage Aware Design	Edith Beigne, LETI, France
15:40	Coffee break	
16:10	Adaptive Architectural Leakage Control Techniques	Joan Figueras, UPC Barcelona, Spain
16:55	Q&A and general discussion	Joan Figueras, UPC Barcelona, Spain Herman E. Maes, IMEC Leuven, Belgium
17:00	Closing	

Organization:

The workshop is organized by edacentrum, Germany and by researchers of the EU Integrated Projects "PullNANO" (PULLing the limits of NANOcmos electronics) and "CLEAN". For further information or registration please send us an e-mail to info edacentrum [dot] de (info@edacentrum.de).

Registration:

Registration is necessary also for CLEAN and PullNANO partners.

For registration please send us an e-mail by clicking the following link info@edacentrum [dot] de

	Until August 24, 2007
non-partners	
Industry	EUR 400,-*
Academia	
Professors	EUR 200,-*
PhD students and students	EUR 100,-*
All prices plus 19 % Sales Tax.	

* Employees, professors and students affiliated with a company, university or research center participating in CLEAN or PullNANO are **free of charge**. These companies, research institutes and universities are CLEAN or PullNANO partners. Their participation cost is covered by the CLEAN and PullNANO project.

Included with a registration are:

- lunch
- coffee breaks
- printed slides binder

Registration deadline is August 24, 2007
Registrations after that deadline will be charged with an additional fee of EUR 50,- (plus 19 % Sales Tax).

You can download the registration form here [2]!

Arrival ...

The main campus of the Technical University Munich (TUM) is situated close to Munich central railway station and benefits from good public transport connections.

Travelling by underground railway

From the central station to the TUM it is about 7 minutes by underground railway. Enter U2 direction: "Feldmoching, München" and leave at the second stop "Theresienstrasse". Back to daylight you will find yourself in "Augustenstrasse" at the location marked with the green flag in the map below. Now you are up to a 5 minutes walk following the blue line in the map until you reach the north entrance (Theresienstrasse 90, red flag) of the TUM. Then please follow the signposts to ESSDERC/ESSCIRC.

For a time table from your preferred underground station to the stop "Theresienstrasse" please follow this link to the online information system

undergound railway time table [3]

Travelling by train

From the central station to the TUM it is about 10 minutes on foot. Keep to the left on leaving the central railway station by the main exit and walk along Luisenstrasse. Cross Brienner Strasse at Königsplatz square, cross Gabelsberger Strasse and continue to Theresienstrasse. Keep to the right until the north entrance (Theresienstrass 90) of the TUM. Then please follow the signposts to ESSDERC/ESSCIRC.

If you prefer to use public transport please follow this link to the online information system. Long-distance trains [3] arrive several times each day in Munich from all over Germany and Europe.

[3]

Travelling by plane

It takes approximately 60 minutes by rail from the Munich International Airport [4] to the central station using the S1 or S8 line.

[5]

Travelling by car

Due to the traffic and parking situation near the campus, we do not particularly recommend driving to the TU München. There are no visitors' parking lots at the main campus. Should you nevertheless decide to travel by car, please bear in mind that you need about 1 hour to travel from the outskirts of the city to the town centre during the rush hour.

Der von Ihnen verwendete Browser wird von der Maps JavaScript API nicht unterstützt. Bitte wechseln Sie zu einem anderen Browser.
Weitere Informationen
Schließen

Größere Kartenansicht [6]

On-demand Training Available

Customized editions of 1 day or 2 days Workshop editions can be organized at customer's site upon request. Please contact the CLEAN web-site for special arrangements and quotations.

About edacentrum GmbH:

The edacentrum GmbH was founded on 1 January 2005 as a wholly-owned subsidiary of the edacentrum e.V., an association of major semiconductor and EDA companies based in or with legal subsidiaries in Germany, including such companies as Infineon, Nokia, Bosch, Atmel, and Philips. The mission of the edacentrum GmbH is to provide individual services in the EDA sector, including consulting, the organization of trainings, Workshops and networking events, the dissemination of information material, and project management. Although the edacentrum GmbH itself is a still young company, its activities are in continuation of the edacentrum e.V., which has successfully established as the German EDA competence centre since its founding in 2001. In CLEAN, edacentrum will participate in training activities (Activity A6).

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CLEAN Participants:

- STMicrolectronics
- Infineon Technologies
- OFFIS - Institut für Informatik
- Politecnico di Torino
- Universitat Politecnica de Catalunya
- CEA-LETI
- Politechnika Warszawska
- ChipVision Design Systems
- BullDAST
- edacentrum GmbH
- Technical University of Denmark
- Consorzio per la Ricerca e l'Educazione Permanente
- Budapest University of Technology and Economics

PullNANO Participants:

- ACIES
- AMO GmbH
- ARCES - UNIVERSITY OF BOLOGNA
- CEA
- Chalmers University of Technology
- CNRS
- ENSERG
- ETH Zentrum
- Europartners legal office
- EUROPEAN COMMISSION
- EUROPEAN SYNCHROTRON RADIATION FACILITY
- Forschungszentrum Juelich
- Fraunhofer-Gesellschaft zur Förderung der angewandten Forschung e.V.
- Freescale
- FZJ
- GÖTEBORGS UNIVERSITET
- IMEC
- IMEP/ENSERG/MINATEC-INPG
- Infineon Technologies AG
- ION BEAM SERVICES
- ISD INTEGRATED SYSTEM DEVELOPMENT S.A.
- IU.NET
- LAHC - Université de Savoie
- MAGWEL NV
- Microwave Lab.
- Université catholique de Louvain
- NATIONAL TECHNICAL UNIVERSITY OF ATHENS
- NXP Semiconductors

- Philips
- Qimonda
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- TECHNISCHE UNIVERSITAET CHEMNITZ
- TUW
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- University of Glasgow
- University of Liverpool
- University of Newcastle upon Tyne
- University of Surrey
- University of Warwick
- Warsaw University of Technology

Perspectives on Technological Options to control leakage in advanced Si CMOS devices

Thomas Hoffmann, IMEC, Belgium

Abstract

To a large extent, scaling was not seriously challenged in the past. However, a closer look reveals that early signs of scaling limits were seen in high-performance devices in recent technology nodes. As conventional scaling becomes power-constrained, innovations in device architecture and/or material are necessary. We will review how those technological changes trade-off in terms of device performance versus power containment.

CV

Thomas Hoffmann (Ph.D.,'00) joined Intel Corporation's R&D group in Hillsboro (OR-USA), as a TCAD engineer for sub-90nm technologies. In 2004, he moved to Intel's technology development group as a device engineer for 45nm process development. In 2005, he joined IMEC in Leuven, Belgium, to lead the electrical characterization group for advanced silicon technologies. He has authored approximately 20 technical papers for publication in journals and presentations at conferences.

High-gate stacks: the solution for leakage reduction?

L. Pantisano, IMEC, Belgium

Abstract

High-k gate stacks are expected to be introduced in the coming 32nm CMOS node. Depending on the application and the leakage requirements (i.e., high-performances or low power operations) a several optimization opportunities are possible. This talk first reviews fundamental properties of the high-k gate stacks and further shows possibilities / limiting factors to achieve high mobility, low leakage and low defect densities, as well as stability after high temperature treatments.

CV

Luigi Pantisano received his Master and PhD in electrical engineering from University of Padova, Padova (Italy) with a thesis on the impact of plasma charging damage on CMOS technologies. In 2000 he was at Bell Labs, Lucent Technologies working on the impact of plasma charging damage on RFCMOS. In 2001 Luigi joined IMEC and he's now a senior scientist in the field of high-k gate stacks. Luigi authored or co-authored more than 120 papers in the field characterization and reliability

Leakage Currents in Nanometer CMOS Devices

Thomas Schulz, Infineon, Germany

Abstract

Various sources of leakage currents are present in modern nanometer CMOS devices. The introduction of novel materials and devices with smaller geometries and more complex layer stacks will increase the number of possible leakage paths in a single device even further. But additionally to the intra device current loss the leakage in between devices and along the periphery components will be more severe, too. This talk reviews different kind of leakage current contributions and possible alternative approaches in device design.

CV

Thomas Schulz received the Dipl.-Ing. and Dr.-Ing. degrees in Electrical Engineering from the Ruhr-University Bochum, Germany, in 1997 and 2001, respectively. In 2000 he joined the Corporate Research Nano Device Group of Infineon Technologies AG in Munich working there on novel device concepts. From 2004 to 2006 he worked in the Multi-Gate-FET project at International Sematech/ATDF in Austin as a member of technical staff of Infineon Technologies North America. Since 2006 he joined device development projects at IMEC in Leuven as a senior staff engineer of Infineon Technologies Leuven.

Thomas authored or coauthored over 40 conference and journal publications and has been awarded over 30 patents in the field device design with others pending.

He is currently working on the assessment of 32nm CMOS technologies including the optimization of Multi-Gate-FET devices and their design for basic circuits.

Leakage and Leakage Variability in nano-CMOS devices

Asen Asenov, University of Glasgow, UK and Jürgen Lorenz, Fraunhofer Institut für Integrierte Systeme und Bauelementetechnologie-IISB, Erlangen, Germany

Abstract

The ongoing miniaturization of nanoelectronic devices leads to various new challenges. Among others, further shrinking gate lengths require the use of advanced device architectures and new materials to achieve the required functionality e.g. in terms of leakage and drive currents. Moreover, "intrinsic" variability associated with discreteness of charge and granularity of matter is now a major factor limiting scaling and integration. Process and device simulation is essential to assess the physical effects occurring and their impact on device and circuit functionality.

In this presentation several examples will be given how simulation contributes to the assessment and solution of these problems. Using coupled three-dimensional process and device simulation, the benefits and drawbacks of bulk CMOS and several transistor architectures which employ SOI material have been analyzed and been optimized in the EC funded project PULLNANO and will be reported. Besides these selected results on device performance and variability, additional results obtained e.g. on the simulation of LER and an outlook on future simulation requirements and approaches will be given.

CV

Asen Asenov received his MSc degree in solid state physics from Sofia University, Bulgaria in 1979 and the PhD degree in physics from The Bulgarian Academy of Science in 1989. In 1989-1991 he was a Visiting Professor at the Physics Department of Technical University of Munich, Germany. He joined the Department of Electronics and Electrical Engineering at the University of Glasgow in 1991, and served as a Head of Department in 1999-2003. As a professor of Device Modeling, Leader of the Glasgow Device Modelling Group and Academic Director of the Glasgow Process and Device Simulation Centre he coordinates the development of 2D and 3D quantum mechanical, Monte Carlo and classical device simulators and their application in the design of advanced and novel CMOS devices. He has pioneered the simulations and the study of various sources of intrinsic parameter fluctuations in decanano- and nano-CMOS devices including random dopants, interface roughness and line edge roughness. He has over 380 publications in process and device modelling and simulation, semiconductor device physics, 'atomistic' effects in ultra-small devices and impact of variations on circuits and systems. Dr Asenov is a fellow of the Royal Academy of Scotland and a member of the IEEE Electron Device Society Technology Computer-Aided Design Committee.

Jürgen Lorenz is head of the Technology Simulation department of the Fraunhofer Institut für Integrierte Systeme und Bauelementetechnologie IISB in Erlangen, Germany. His main subjects are the development of physical models and programs for semiconductor process simulation and the required algorithms. He has so far been involved in 23 European projects, among which he has coordinated 7 on developments for process simulation and on specifications for TCAD.

Following requests from industry he contributes since 2000 as expert to the preparation of the International Technology Roadmap on Semiconductors, and has been chairman for its Modeling and Simulation Chapter since 2002.

Leakage reduction in sub-100nm CMOS Technologies: Bridging the Gap between Technology, Circuit Design and Product Requirements

Christian Pacha, Infineon Technologies, Munich, Germany

Abstract

With the introduction of the 90nm CMOS technology node leakage reduction techniques became an essential topic of circuit and system design to meet product requirements. Using a 90nm CMOS mobile phone baseband processor as case study for a typical portable low power product, this talk will give an overview of implemented leakage reduction techniques from an industrial perspective. Since the efficiencies of leakage reduction techniques are strongly depending on CMOS device properties and available technology options, the interrelation between technology and circuit design is analyzed. Moreover, the trade-offs between leakage reduction factors, area increase, design effort, and impact on product performance are discussed considering overall power management aspects and typical application requirements. As an outlook the scalability of leakage reduction and low power circuit techniques are assessed based on preliminary 45nm CMOS and Multi-Gate FET based CMOS circuit results.

CV

Christian Pacha received the Dipl.-Phys. and Dr.-Ing. degrees from the University of Dortmund, Germany, in 1996 and 2001, respectively. From 1996 to 2000, he was with the Department of Microelectronics, University of Dortmund, where he investigated circuit concepts for resonant tunnelling devices. Since 2000, he has been with Infineon Technologies, Corporate Research, Munich, Germany. In 2005, he joined the Business Group Communication Solutions as team leader for technology-oriented circuit design at the Advanced Systems and Circuits department. He is currently working in the fields of low-power circuit design, impact of process variations on SoC architectures, and circuit exploration of nanometer-scaled CMOS devices, including 45 nm CMOS technologies and Multi-Gate FET devices. He has authored or co-authored more than 25 technical publications.

Invited Keynote: High Level Energy and Power Reduction Strategies

Christian Piguet, CSEM, Switzerland

Abstract

As leakage power and total power is a more and more dramatic issue is very deep submicron technologies, this talk explores new design methodologies for designing digital architectures presenting the lowest total power consumption (so static and dynamic power) or the lowest total energy for a given task. A relationship between leakage power due to very advanced technologies and high-level architectures is performed based on architectural parameters like activity, logical depth, number of transitions for achieving a given task and total number of gates. Various architectures for a same logic function are compared at very low Vdd and VT that define the optimal total power consumption of each architecture. The optimal energy is generally obtained with subthreshold implementations. Various design method are presented, like selection of the best architecture from a set of architectures (baseline, sequential, parallel, pipelined, etc..) at optimal Vdd and threshold voltages, or like a design method that takes as constraints predefined Vdd and threshold voltages.

CV

Christian Piguet received the M. S. and Ph. D. degrees in electrical engineering from the Ecole Polytechnique Fédérale de Lausanne, respectively in 1974 and 1981. He joined the Centre Electronique Horloger S.A., Neuchâtel, Switzerland, in 1974. He is now Head of the Ultra Low Power Circuits section at the CSEM Centre Suisse d'Electronique et de Microtechnique S.A. He is presently involved in the design of low-power low-voltage integrated circuits in CMOS technology, including design methodologies, microprocessor architectures and logic design. He is Professor at the Ecole Polytechnique Fédérale Lausanne (EPFL), Switzerland, lectures in VLSI and microprocessor design at the University of Neuchâtel, Switzerland and in the ALaRI master at the University of Lugano, Switzerland. Christian Piguet holds 32 patents in digital design, microprocessors and watch systems. He is author and co-author of more than 190 publications in technical journals and of books and book chapters in low-power digital design.

Circuit Level Leakage Aware Design

Edith Beigne, LETI, France

Abstract

As technology is scaled, circuits have to be more and more power effective either in terms of dynamic power or in terms of leakage.

This presentation will deal with design techniques to reduce leakage power and dynamic power taking into account SoC considerations.

We will first focus on state of the art, explaining existing techniques at design level either "full custom" or tools driven. The second part will present a real realization implementing different design techniques and should lead designers to make choices depending on their circuit and power saving constraints they have.

CV

Edith Beigné received the Electronic Engineering Diploma from the National Polytechnic Institute of Grenoble, France, in 1998.

In 1998, she joined the CEA-LETI laboratory in the Center for Innovation in micro & nanotechnology (MINATEC), Grenoble. She was first involved in contacless RFID mixed signal systems. In 2001, she began the asynchronous logic design activity in cryptographic and contacless systems. Around the development of the FAUST project, she has designed a part of the asynchronous Network-On-Chip. Since 2006, she is in charge of ALPIN, a power aware GALS SoC implementing dynamic and static low power techniques based on an asynchronous NoC.

Adaptive Architectural Leakage Control Techniques

Joan Figueras, UPC Barcelona, Spain

Abstract

As technology is scaled in the nanometric range the variability of the manufacturing process on the circuit parameters becomes critical. The classical "design margin" approach to compensate for uncertainty becomes ineffective and costly. An emerging design paradigm consists in the provision of "on-chip adaptivity" to compensate dynamically to variability (Process parameters, Voltage and Temperature).

In this module the architectural trends to adaptively control leakage power will be explored. To reduce subthreshold leakage currents Adaptive Body Bias (ABB) has been used, however its efficiency for technologies with increasing tunneling currents becomes less efficient. Adaptive Supply Voltage (ASV) used to control active as well as leakage power will be presented. The combination of ASV and ABB permits to adapt the system to reduce power maintaining its highest frequency of operation. Architectural solutions based on Adaptive Source Bias (ASB) in SRAMs without loosing the memory state in stand-by are becoming promising strategies to adaptively reduce leakage.

CV

Dr. Figueras obtained his Engineering Degree at the ETSEIB of the Universitat Politècnica de Catalunya and his MsC and PhD degrees from the University of Michigan in Ann Arbor. Currently, he works at the Engineering Dpt. of the UPC with research and teaching responsibilities in the area of Electronics, Digital and Mixed-Signal Design and Test. His research interests are centered in emerging topics in low power design and advanced test of electronic circuits and systems. He has an extensive publication record and has presented seminars and tutorials in professional meetings, NATO seminars on topics related to "Low Power Design" and "Quality in Electronics". He is currently vice-chair of the IEEE Test Technology Technical Council, editor of JETTA, and member of steering and program committees of several Test and Low Power Design Conferences.

Quell-URL: https://www.edacentrum.de/controlling-leakage-power-nanometer-cmos-technology-meets-design

Links:
[1] https://www.tum.de/
[2] https://www.edacentrum.de/system/files/files/veranstaltungen/2007/controlling-leakage-power/clean-pullnano-workshop-munich-2007.pdf
[3] http://reiseauskunft.bahn.de/bin/query.exe/en?searchMode=ADVANCED&S=&start=1&Z=M%FCnchen%20-%20Maxvorstadt%2C%20Theresienstr.%2090&ZADR=1&date=14.09.2007&time=08%3A30×el=arrive
[4] http://www.munich-airport.de
[5] http://reiseauskunft.bahn.de/bin/query.exe/en/dn?searchMode=ADVANCED&S=München%20Flughafen%20Terminal&start=1&Z=München%20-%20Maxvorstadt,%20Theresienstr.%2090&ZADR=1&date=14.09.2007&time=08%3A30×el=arrive
[6] http://maps.google.de/maps?f=q&source=embed&hl=de&geocode=&q=Theresienstr.+90,+80333+M%C3%BCnchen&aq=&sll=51.151786,10.415039&sspn=18.809516,37.089844&vpsrc=0&ie=UTF8&hq=&hnear=Theresie