Analog design automation : dream or reality ?

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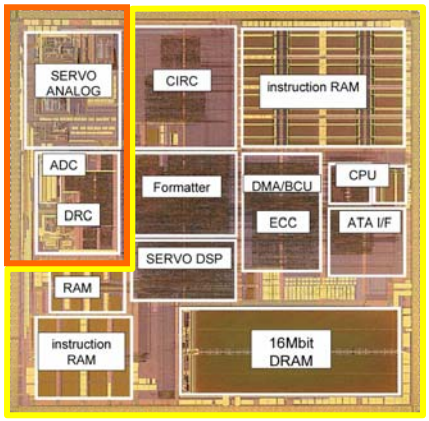
Contents

- **motivation and context**
- simulation and modeling techniques for design and verification
- circuit and layout synthesis
- signal integrity and reliability analysis
- conclusions

An historical note

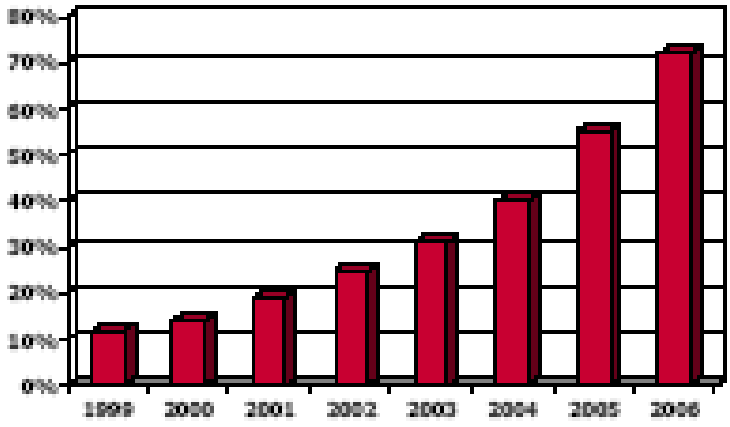
- **today's reality is different though …**



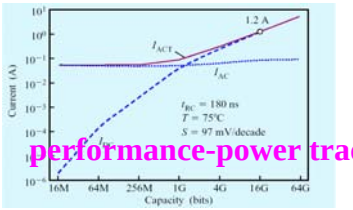
- ❑ **increased design complexity challenges design and verification methodologies**
- ❑ **tightening time-to-market constraints challenge analog design productivity**
- ❑ **embedding mixed-signal/RF blocks with digital causes signal integrity hazards**

The future is mixed-signal

- **% SOCs with analog components :**

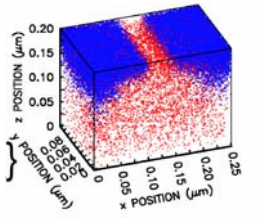


Enter the nano CMOS era

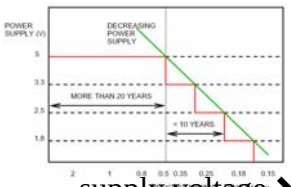


performance-power trade-off

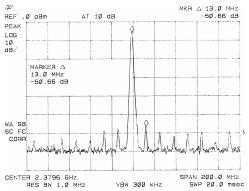
leakage power ↗



variability ↗



supply voltage ↘



signal integrity ↗

+ new materials

+ new devices (e.g. FinFETs)

+ new degradation mechanisms

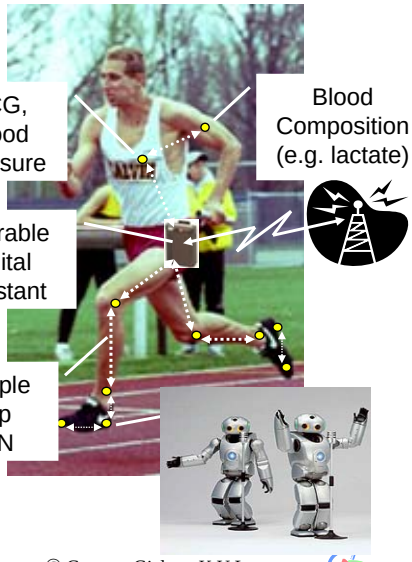
4G wireless systems

- **software-defined radio – cognitive radio**

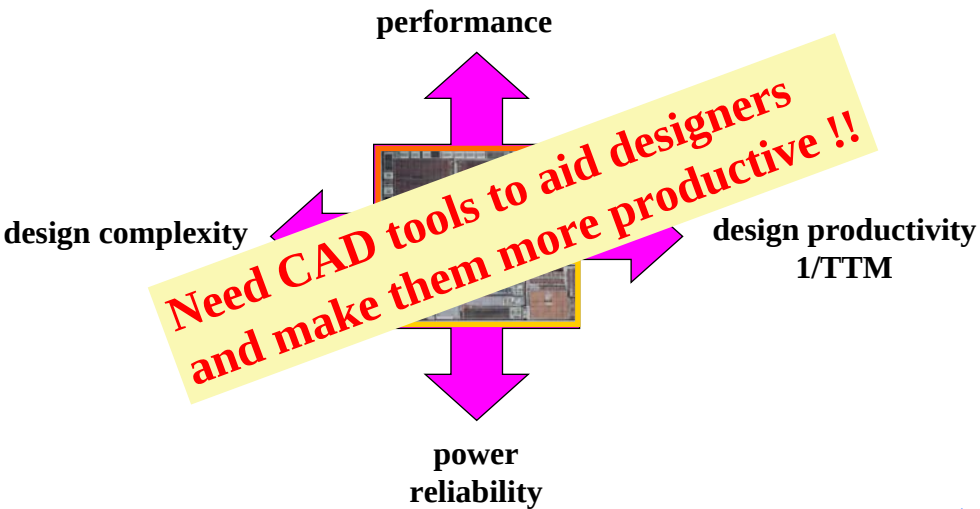
reconfigurability, feedback loops, calibration, etc.

Wireless sensor networks

- Smart home
- Medical applications and health care
- Energy management
- Logistics : tracking, locationing...
- Traffic & transport
- Emergencies / security / safety
- Entertainment
- Wellbeing – human comfort



The designer's dilemma



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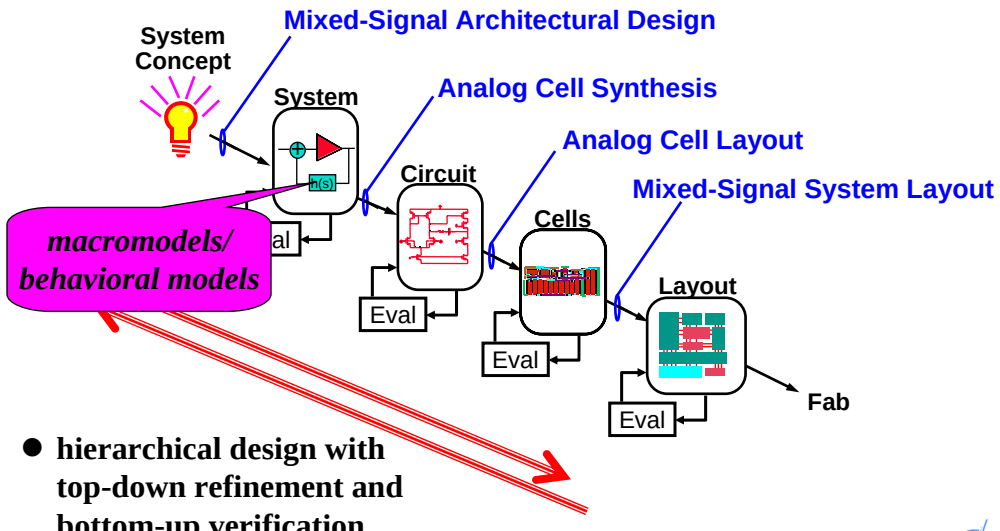
Mixed-signal system design flow



- **hierarchical design with top-down refinement and bottom-up verification**

Analog behavioral models

a *behavioral model* of an analog circuit is a mathematical description that approximates the input-output behavior of the circuit

- describe **behavior** of the circuit; not internal netlist
  - combination of procedures/differential/algebraic equations, transfer functions
  - examples : $V_{out} + \frac{1}{p_1}\frac{dV_{out}}{dt} = A_o(V_{in+} - V_{in-})$ $\quad V_{out} = \sin(2\pi\int_0^t (f_{ref} + g(v_{in} - v_{ref}))dt)$
- includes **first-order behavior,** but also **major nonidealities**
- models can be described in standardized VHDL-AMS and VERILOG-AMS
- **key problem is the (computer-aided) model generation** !!

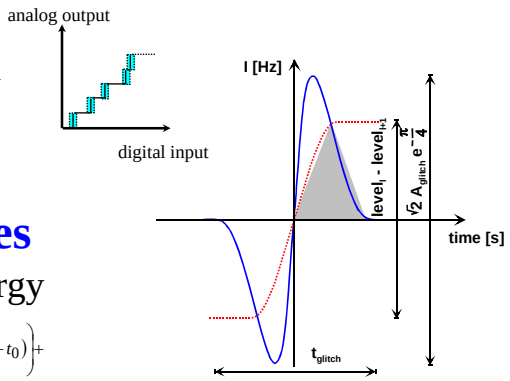
Example : current-steering DAC

- **model as a functional block**
- **static nonidealities**
  - model the transition points
  - INL and DNL are statistical

    $t \sim normal(\mu_t, \Sigma_t)$

    $t = \mu_t + U_t c_t \;\; , \;\; c_t \sim normal(0, \Sigma_{ct})$
  - error signatures

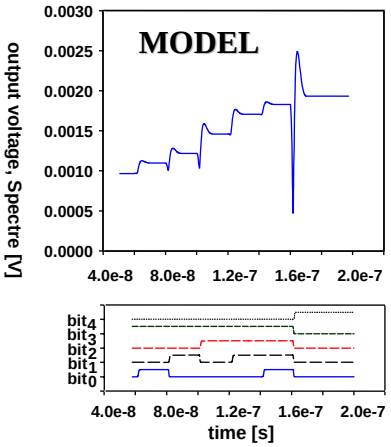
[Vandenbussche TCAS-II 2001]

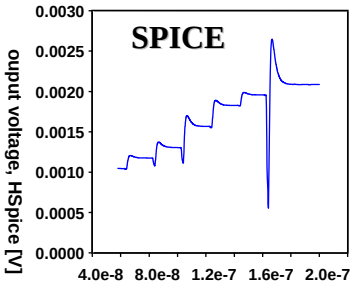


- **dynamic nonidealities**
  - settling time, glitch energy

$$i_{out} = A_{gl}\sin\left(\frac{2\pi}{t_{gl}}(t-t_0)\right)\exp\left(-sign(t-t_0)\frac{2\pi}{t_{gl}}(t-t_0)\right) + \frac{level_{i+1} - level_i}{2}\tanh\left(\frac{2\pi}{t_{gl}}(t-t_0)\right) + \frac{level_{i+1} + level_i}{2}$$

Example : current-steering DAC

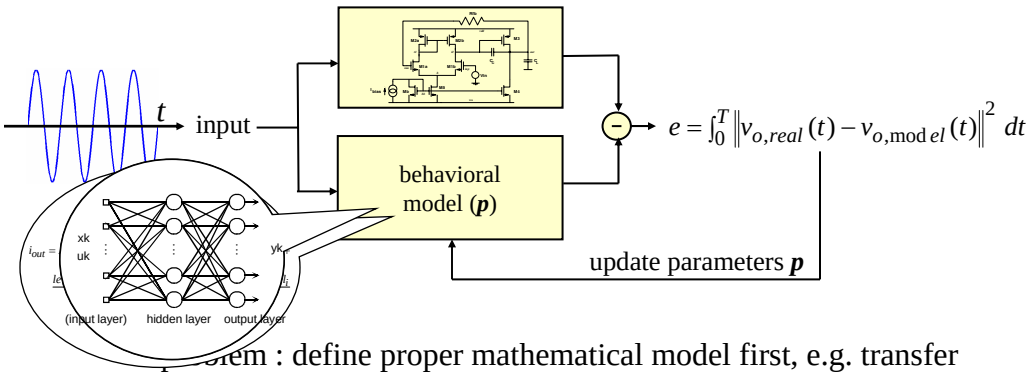




error : <1%
speed-up : 874 x !!

Generation of behavioral models

- **regression approach :**
  fit simulation results to predefined template
  - ❒ least square fit to mathematical model,



problem : define proper mathematical model first, e.g. transfer function, or artificial neural network…

(Non)linear model order reduction

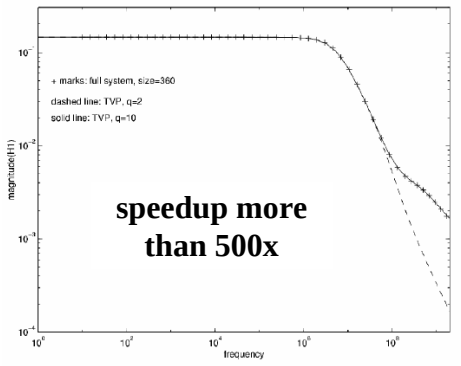
- originally : interconnect modeling
- now : (non)linear circuit modeling

$$\mathbf{E}\frac{d\mathbf{x}}{dt} = \mathbf{A}\mathbf{x} + \mathbf{b}\mathbf{u}$$
$$\mathbf{y} = \mathbf{C}\mathbf{x} + \mathbf{D}\mathbf{u}$$

order ~ 1000-10,000

$$\overline{\mathrm{E}}\frac{d\mathrm{x}}{dt} = \overline{\mathrm{A}}\mathrm{x} + \overline{\mathrm{b}}\mathrm{u}$$
$$\mathrm{y} = \overline{\mathrm{C}}\mathrm{x} + \overline{\mathrm{D}}\mathrm{u}$$

order ~ 10-100



speedup more than 500x

[Roychowdhury Univ. Minnesota]

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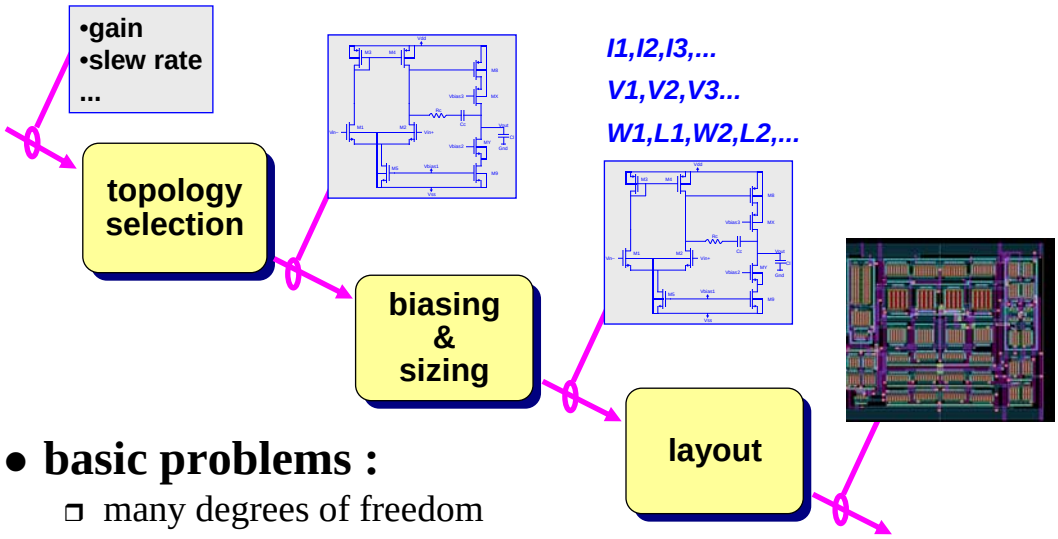
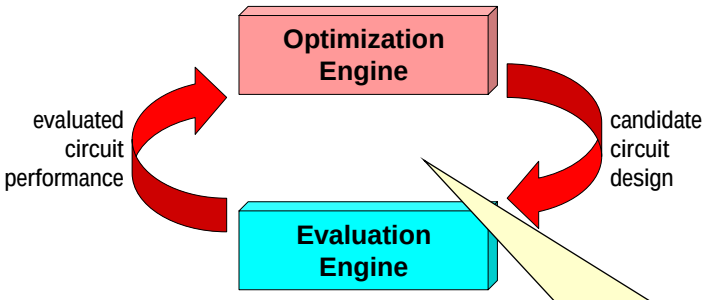
Analog circuit design steps



- **basic problems :**
  - many degrees of freedom
  - many complex trade-offs

Optimization-based sizing

- **most approaches have this structure :**

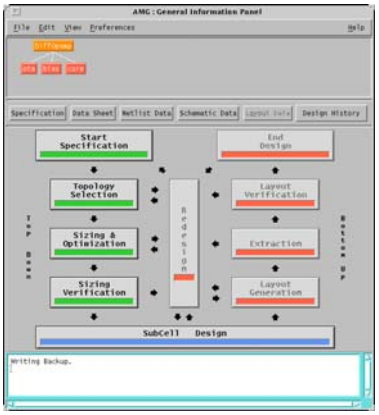


- **cost-based numerical search**
  - cost metric represents "goodness" of
  - different optimization algorithms, e.g.
  - evaluation by simulations and/or equations

- meet performance constraints : $P_i \geq \Psi_i$ or $P_j \leq \Psi_j$
- minimize objectives, e.g. power consumption

AMGIE : circuit & layout synthesis tool

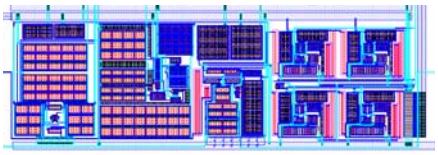
AMGIE



[Van der Plas TCAD 2001]

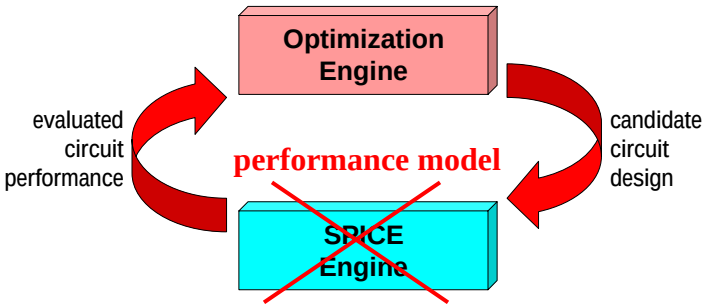
- **covers complete design flow from spec to layout :**
  - optimally tailors circuit to each application and process
  - increases analog design productivity
  - for frequently used cells
    e.g. opamps, filters, Δ-Σ conv...

LAYLA



Performance modeling

- **replace circuit simulations by model evaluations**



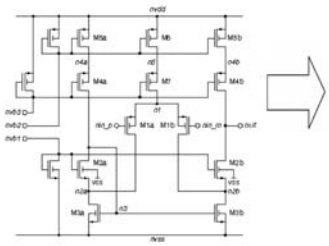
  - performances in terms of design variables

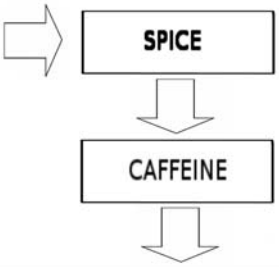
$$GBW = u(V_{bias}, I_{bias} \ldots W, L, R, L, C)$$

  - based on industrial device models (BSIM 3v3, MM11…)
  - both linear and nonlinear characteristics

CAFFEINE : performance modeling

[McConaghy DATE 2005]

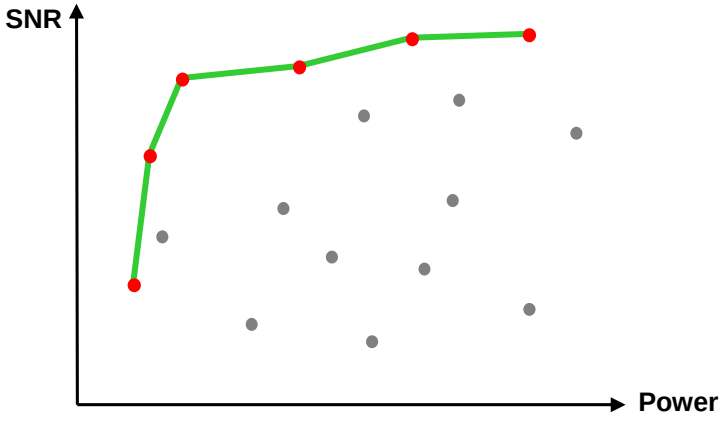




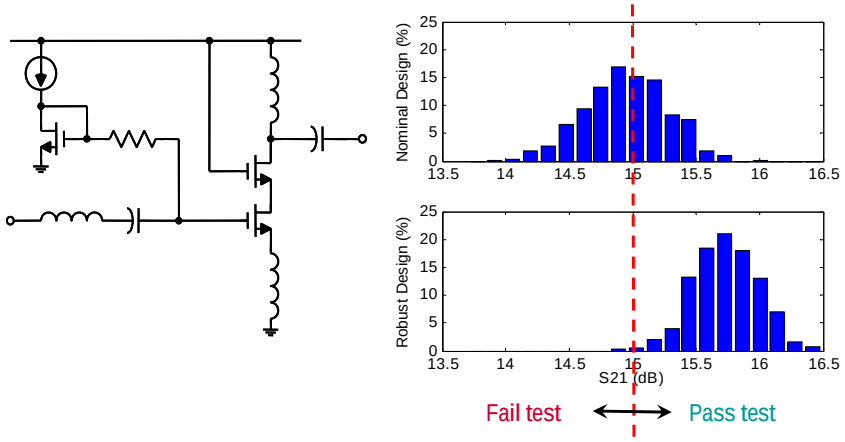
Perf.	Expression
A_{LF}	-10.3 + 7.08e-5 / id1 + 1.87 * ln(-1.95e+9 + 1.00e+10 / (vsg1*vsg3)+ 1.42e+9 *(vds2*vsd5) / (vsg1*vgs2*vsg5*id2))
f_u	10^(5.68 - 0.03 * vsg1 / vds2 - 55.43 * id1+ 5.63e-6 / id1)
PM	90.5 + 190.6 * id1 / vsg1 + 22.2 * id2 / vds2
V_{offset}	- 2.00e-3
SR_p	2.36e+7 + 1.95e+4 * id2 / id1 - 104.69 / id2 + 2.15e+9 * id2 + 4.63e+8 * id1
SR_n	- 5.72e+7 - 2.50e+11 * (id1*id2) / vgs2 + 5.53e+6 * vds2 / vgs2 + 109.72 / id1

Multi-objective optimization

- **handles conflicting performances; generates Pareto-optimal trade-off curves**

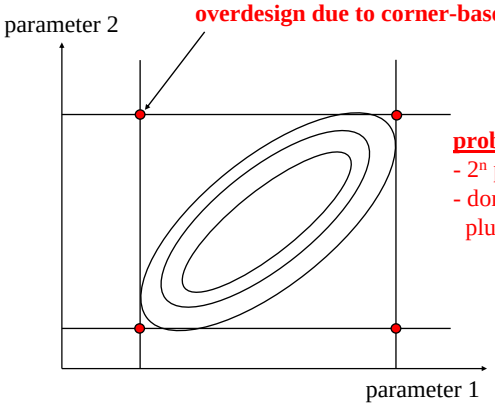


Effect of P,V,T variations



P,V,T variations (including mismatch) limit yield / C_{pk}

Problems with corner-based design

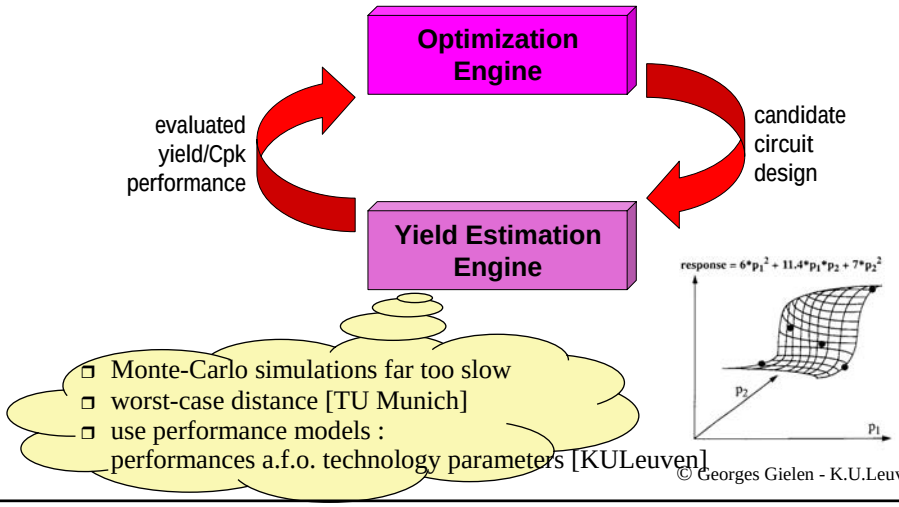


problems for analog circuits:
- 2^n possible corners with n parameters
- don't know which corner is worst for analog circuit plus this can be topology/performance specific

➔ **need statistical design to find real 3(6)-sigma design solution for each circuit**

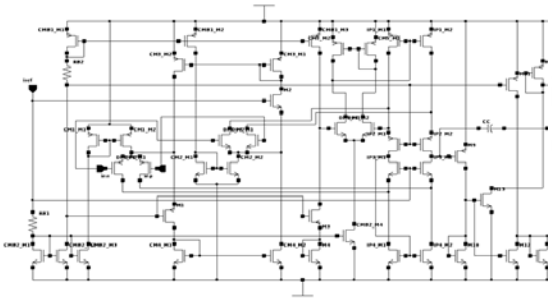
Yield optimization

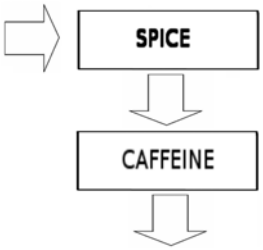
- **yield estimation inside optimization loop to determine optimal biasing/sizes for which yield/C_{pk} is maximal**



- Monte-Carlo simulations far too slow
- worst-case distance [TU Munich]
- use performance models : performances a.f.o. technology parameters [KULeuven]

Using CAFFEINE to create RSMs





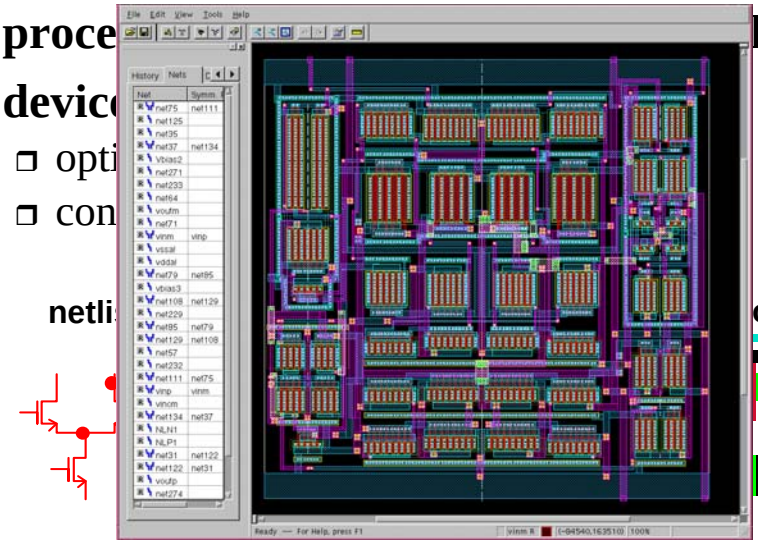
Cpk = 1231.4
- 9.39e+08 * dp2_w^2 *$\sqrt{}$dp1_w * min(6.60e+07 - 76.9 /$\sqrt{}$Cc, 0.104)
+ 1.21e+12 / min(1e+10 - 2.48e-05/($\sqrt{}$dp2_w * Cc), -4.96e+06)
- 0.0012 / $\sqrt{}$Cc + 4.21e+06 * mt4_w^2 / mt1_w

[McConaghy ICCAD 2006]

Analog circuit layout synthesis

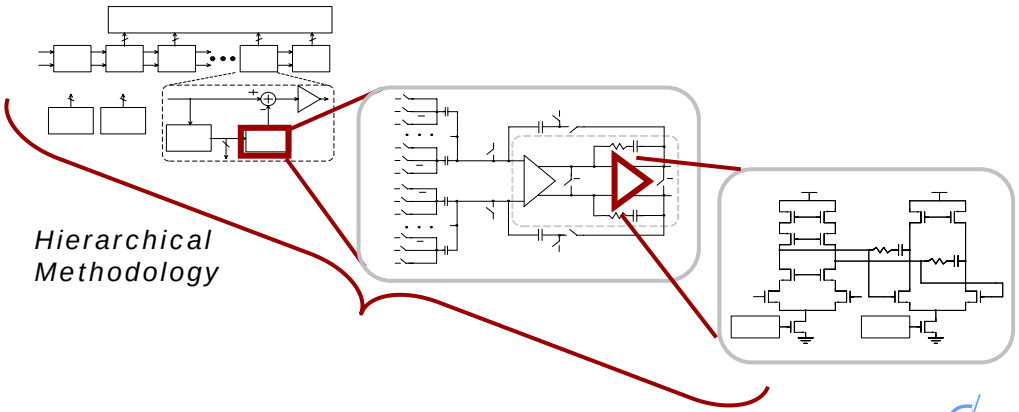
- proce ls")
- devic
  - opti
  - con

netli oute



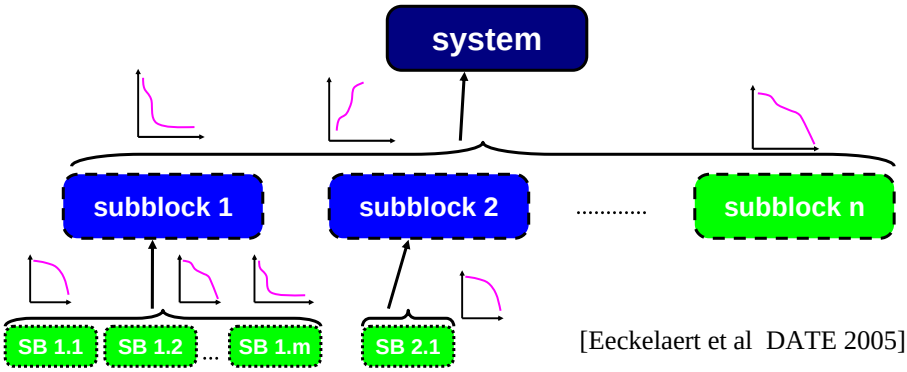
How to optimize complete systems ?

- use a hierarchy of abstractions
  - abstract & behavioral at the top, moving towards real circuits at the bottom



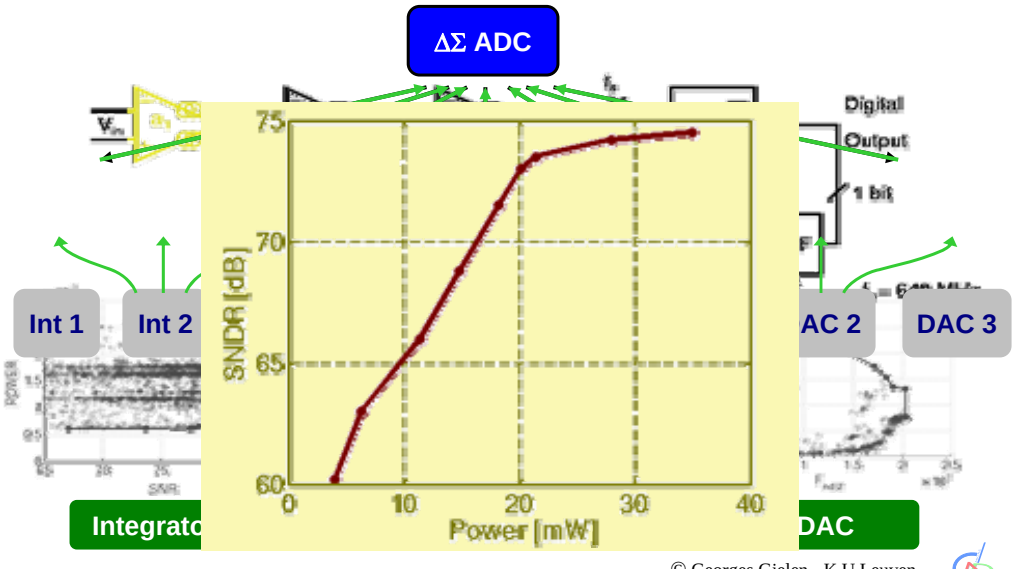
Multi-objective bottom-up synthesis

- **pass "boundary" information up the hierarchy**
  - Pareto surfaces of performance models of subblocks
  - combine information to optimize at higher level

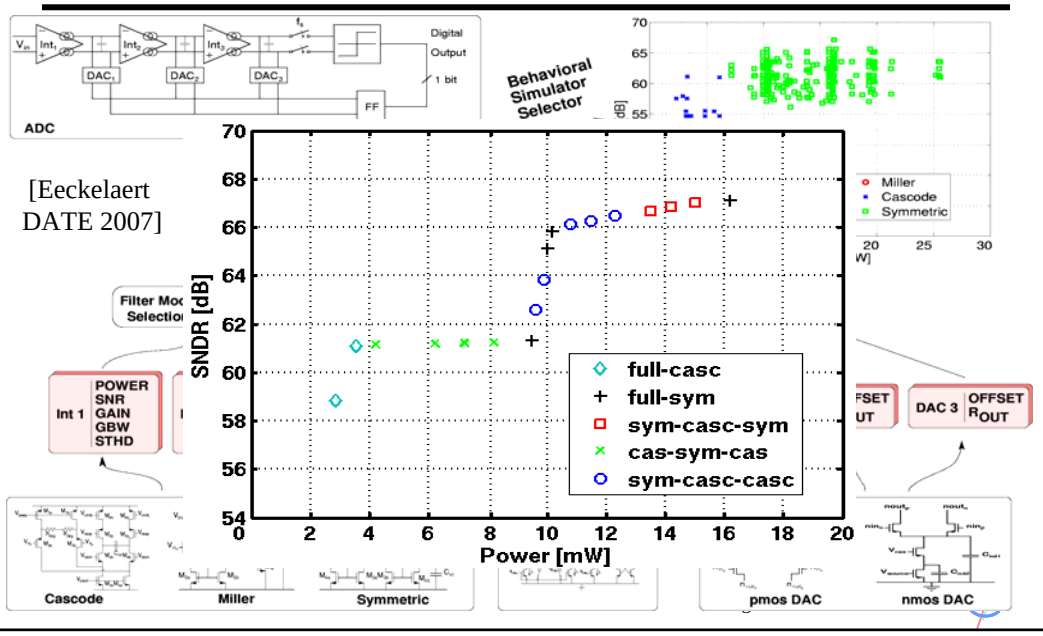


[Eeckelaert et al DATE 2005]

Example : CT Δ–Σ converter



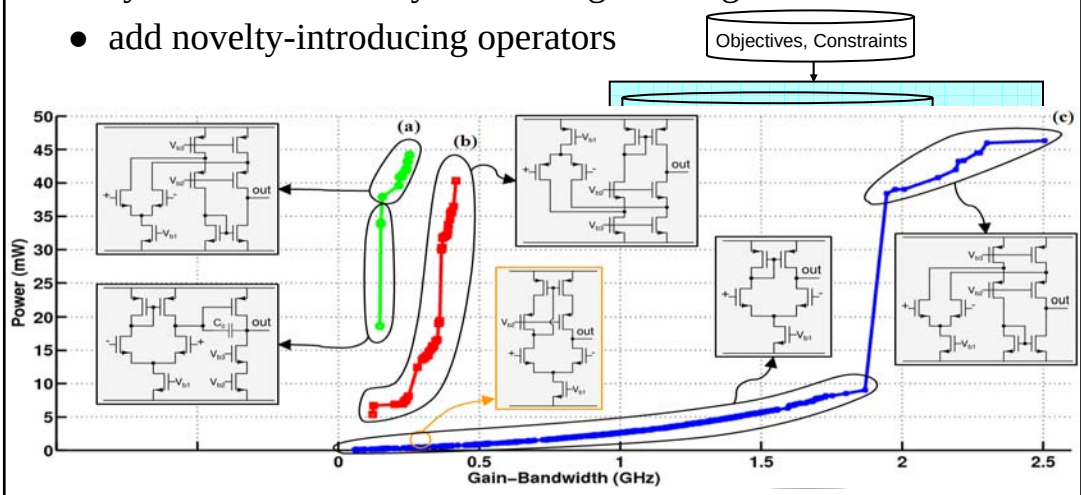
Sizing + topology exploration



[Eeckelaert DATE 2007]

Topology synthesis

- synthesizes circuit by assembling building blocks
- add novelty-introducing operators



[McConaghy DAC 2007]

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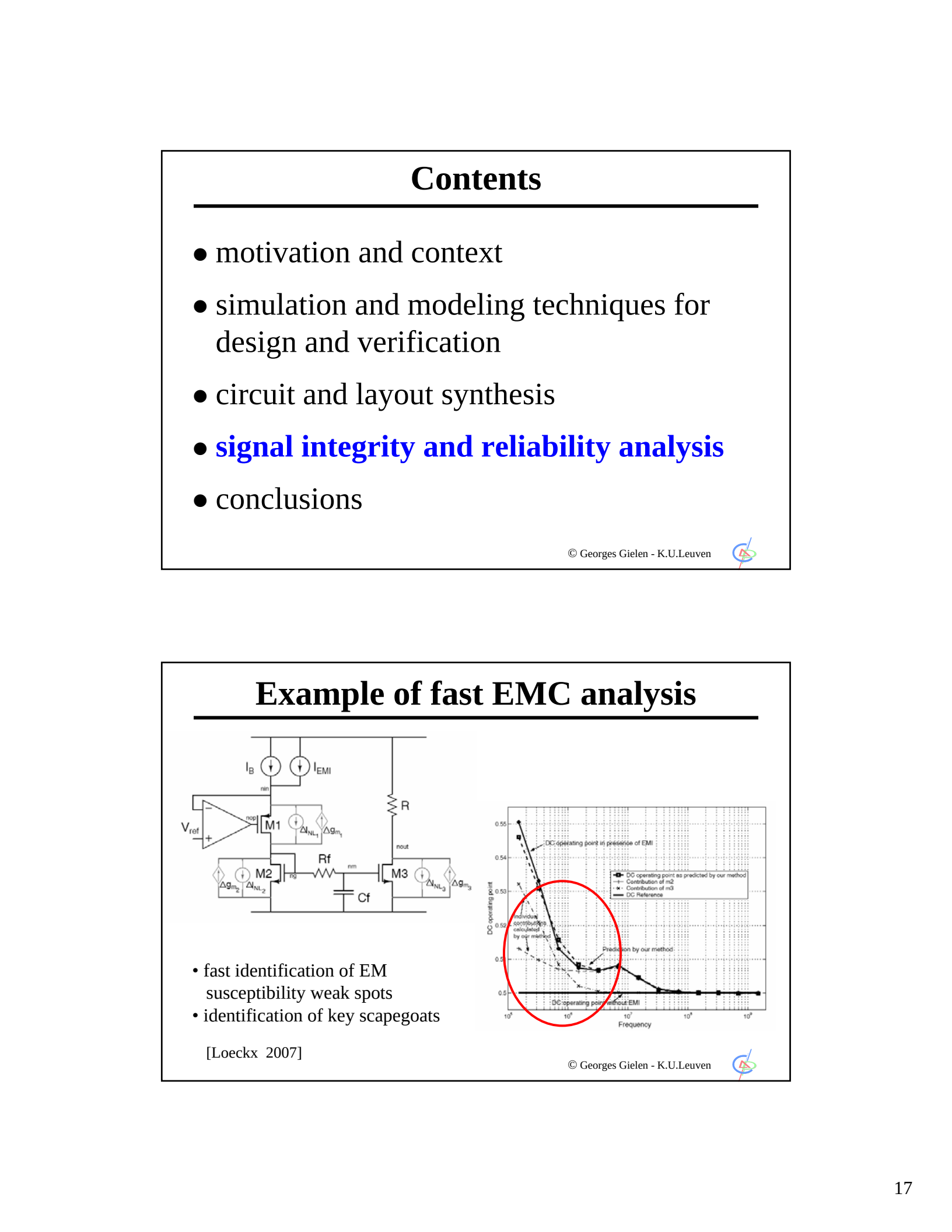


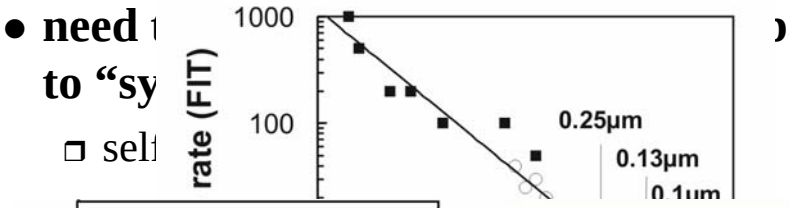
Example of fast EMC analysis

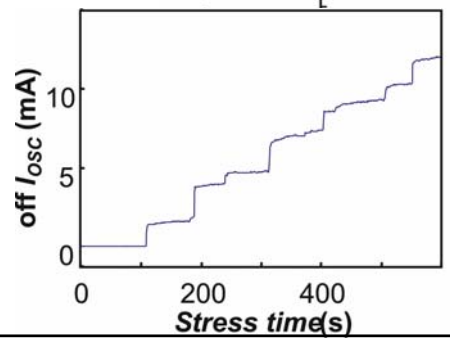
- fast identification of EM susceptibility weak spots
- identification of key scapegoats

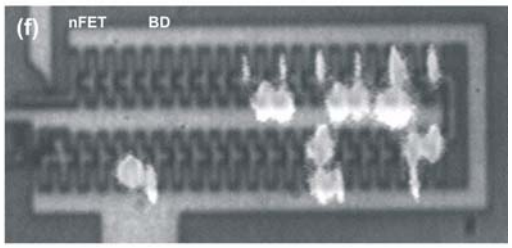
[Loeckx 2007]

Reliability and degradation

- **performance changes over time, until broken**
- **need t … pagate up to "sy**
  - sel…







Conclusions

- **SoC/SiP designs require solution for managing complexity and productivity**
  - nanometer CMOS poses additional challenges
- **design methodologies/CAD tools help analog designers survive**
  - large advances in simulation methods
  - behavioral/macro modeling for top-down refinement and bottom-up system verification
  - analog circuit sizing tools generate optimized designs
  - layout synthesis tools automates layout
  - start on topology synthesis
  - signal integrity and reliability analysis tools pinpoint weak spots in the design