Tuesday
March 11, 2008

10:00 – 12:00 Test, Yield and Costs	
University of Limerick	Data Converter BIST Solutions
University of Bremen	SC_refine
University of Siegen	CostMoS-G
University of Bremen	Crosstalk ATPG
University of Bremen	Crosstalk test compaction

12:00 – 14:00 Bringing Ideas into FPGAs	
Technical University of Braunschweig	FlexFilm
Ulm University	Submarine Explorer
University of Erlangen-Nuremberg	WPPA
University of Pisa	SHINE
Eindhoven University of Technology	PreMaDonna

14:00 – 16:00 System Exploration and Transaction Level Modelling	
RWTH Aachen University	MPSoC Exploration Technique
University of Tehran	TLM Synthesis Studio
Université de Bretagne Sud	Lightweight
Université de Bretagne Sud	GAUT
Université de Bretagne Sud	SoftExplorer
Osaka University	SoC Architecture Explorer
KU Leuven	Coffee

16:00 – 18:00 Software and Hardware in the System	
Université de Bretagne Sud	PALMYRE
Eindhoven University of Technology	CoMPSoC
University of Paderborn	Hardware-in-the-Loop Simulations
University of Paderborn	General Purpose VLIW Processor
Université de Bretagne Sud	µSPIDER
Darmstadt University of Technology	Self-reconfigurable Video processing

10:00 – 12:00 Test, Yield and Costs

University of Limerick, Ian Grout See Day 3
CMOS Implementation for Data Converter BIST/BOST

University of Bremen, Christian Genz
A graphical SystemC refinement tool
We present a graphical design tool that supports the manual refinement of SystemC models with focus on the following features. Separation of HW/SW partitions encapsulated in distinct hierarchies. Highlighting of synthesizable and non-synthesizable fragments of the design.

University of Siegen, Michael Wahl See Day 2.
Design Cost Controlling

University of Bremen, Kishore Duganapalli
GA based ATPG Tool for Crosstalk Induced Logic Faults between On-chip Aggressor and Victim
The ATPG tool proposed here based on Genetic Algorithm, reads the circuit description and generates test patterns for the given set of aggressors and victims in DSM chips.

University of Bremen, Shehzad Hasan
Test Compaction of Crosstalk Faults through Fault List Reordering
An algorithm is proposed for generating test patterns that produce maximal crosstalk effect on any interconnect of a circuit using existing ATPG tool and coupling influence between interconnects.

12:00 – 14:00 Bringing Ideas into FPGAs

Technical University of Braunschweig, Henning Sahlbach, Sean Whitty
See Day 2.
FlexFilm: Real-time digital film processing with a FPGA-based reconfigurable platform

Ulm University, Frank Slomka See Day 2
Submarine Explorer – A low cost AUV

University of Erlangen-Nuremberg, Dmitrij Kissler
A High-Speed Dynamic Reconfigurable Multilevel Parallel Architecture
The CoMap project investigates the holistic co-design of a new class of highly parameterizable, massively parallel processor architectures. Two DSP algorithms were implemented with the help of dynamic reconfiguration on the same WPPA hardware, prototyped on FPGA.

University of Pisa, Luca Fanucci
SHINE: FPGA prototyping of SpaceWire IP cores for High Data Rate and Fault Tolerant Invehicle Networking
An FPGA is programmed with an 8-port SpaceWire Router IP core featuring an AMBA AHB interface. The router is controlled by a PC through a bridge.

Eindhoven University of Technology, Akash Kumar
PreMaDonna: Predictable Matching of Demands on Networked Architectures
We demonstrate a methodology to generate multiprocessor systems-on-chip from the high-level description of applications, namely synchronous dataflow graphs. Attendees will get an opportunity to experiment with this framework and generate multi-processor designs.

14:00 – 16:00 System Exploration and Transaction Level Modelling

RWTH Aachen University, Torsten Kempf See Day 3
An ESL Workbench for early MPSoC Design Space Exploration

University of Tehran, Mahshid Sedghi
TLM Synthesis Studio
TLM Synthesis Studio is an environment to help system level designers start the design and implementation of their systems from transaction level. It supports OSCI TLM library and SystemC. It also provides the designers with a library of configurable TLM components.

Université de Bretagne Sud, Philippe Coussy See Day 3
GAUT – A High-Level Synthesis tool for DSP applications

Université de Bretagne Sud, Pierre Bomel See Day 3
A lightweight and remote partially reconfigurable platform

Université de Bretagne Sud, Johann Laurent
SoftExplorer
SoftExplorer is a power/energy estimation tool that is developed into the Low Power Design Group of the LESTER laboratory. This tool allows the programmer to rapidly estimate the power and energy consumption of its application executed on a processor. SoftExplorer owns several power models of processors.

Osaka University, Ittetsu Taniguchi See Day 2
SoC Architecture Explorer

KU Leuven, Andy Lambrechts
The Coffee framework: COmpiler Framework for Energy-aware Exploration
Modern mobile devices need to be extremely energy efficient. This demo presents a unified optimization and exploration framework, from source level transformation to processor architecture design.

16:00 – 18:00 SW and HW in the System

Université de Bretagne Sud, Pierre Bomel See Day 3
A mixed (hardware and software) rapid prototyping platform.

Eindhoven University of Technology, Andreas Hansson See Day 3
CoMPSoC - A Composable and Predictable Multi-Processor System-on-Chip Template

University of Paderborn, Christopher Pohl See Day 3
Hardware-in-the-Loop Simulations with Matlab/Simulink/ModelSim for FPGA based designflows

University of Paderborn, Thorsten Jungeblut See Day 3
General Purpose VLIW Processor for Multiband-Multistandard applications

Université de Bretagne Sud, Rachid Dafali See Day 2
µSPIDER CAD TOOL: CASE STUDY OF NOC IP GENERATION FOR FPGA

Darmstadt University of Technology, Kurt Ackermann
Demonstration of a Self-Reconfigurable Video-Processing Frame-grabber
Limitations of logic and RAM resources of FPGAs are bottlenecks for many complex algorithms. Partitioning of complex algorithms in smaller sequentially reconfigured and executed units makes smaller FPGA devices suitable. We show a video processing framegrabber, connected to a high resolution matrix camera for a complex self-reconfigurable design on a Virtex-4 board.

Wednesday, March 12, 2008

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10:00 – 12:00 Mixed Signal Design, Test Solutions and More	
RWTH Aachen University	MPSoC Exploration Technique
University of Limerick	Data Converter BIST Solutions
Technical University of Braunschweig	FlexFilm
University of Siegen	CostMoS-G
University of Southampton	CATS
Fraunhofer-Institut für Techno- und Wirtschaftsmathematik	Analog Insydes

12:00 – 14:00 System Analysis, Simulation and Verification	
Fraunhofer-Institut für Techno- und Wirtschaftsmathematik	Analog Insydes
University of Bremen	SC_refine
Ulm University	Submarine Explorer
University of Tokyo	FLEC
University of Newcastle upon Tyne	Workcraft

14:00 – 16:00 SoC, Platforms and SystemC	
University of Tehran	TLM Synthesis Studio
Université de Bretagne Sud	SoftExplorer
Osaka University	SoC Architecture Explorer
Université de Bretagne Sud	µSPIDER
Eindhoven University of Technology	SDF3
University of Bonn	ReChannel
Chemnitz University of Technology	SpecScribe
Universität Karlsruhe	MORPHEUS

16:00 – 18:00 Hardware Solutions	
Université de Bretagne Sud	Lightweight
Université de Bretagne Sud	GAUT
Université de Bretagne Sud	PALMYRE
Universidad Complutense de Madrid	Wireless Body Area Network
Eindhoven University of Technology	CoMPSoC
University of Bonn	FFTS
Technical University of Denmark	Model based HW verification
University of Rostock	IPclip

10:00 – 12:00 Mixed Signal Design, Test Solutions and More

Technical University of Braunschweig, Henning Sahlbach, Sean Whitty
FlexFilm: Real-time digital film processing with a FPGA-based reconfigurable platform
The FlexFilm board is a reconfigurable platform based on four Virtex II Pro FPGAs. Several run-time reconfigurable algorithms for real-time digital film processing for resolutions up to 2048x1556 pixels@24 FPS in 10-Bit RGB are demonstrated. The system achieves a sustained performance of 170 GOPS.

RWTH Aachen University, Torsten Kempf See Day 3
An ESL Workbench for early MPSoC Design Space Exploration

University of Limerick, Ian Grout See Day 3
CMOS Implementation for Data Converter BIST/BOST

University of Siegen, Michael Wahl
Design Cost Controlling
CostMoS-G is a tool for collaborative work on cost optimal designs. The user (designers, managers, and controllers) can define arbitrary cost models for the products life cycle. Monte-Carlo simulation allows dealing with value ranges, and the integrated time model permits cost predictions for future reviews.

University of Southampton, Reuben Wilcock
Post Manufacture Variability Improvement Using Configurable Analogue Transistors (CATs)
Analogue design is becoming a bottleneck due to increased process variability. A configurable analogue transistor structure is proposed which allows post manufacture adjustment. The demonstrator shows live results from a silicon prototype, highlighting the adjustability and improvement offered by this approach.

Fraunhofer-Institut für Techno- und Wirtschaftsmathematik, Jochen Broz
Behavioral Modeling using Analog Insydes
Analog Insydes is a tool for modelling and analyzing analog circuits symbolically. For handling model complexity, it provides the methodology of symbolic approximation which is an innovative model-order reduction technique.

12:00 – 14:00 Sys. Analysis, Simulation and Verification

Ulm University, Frank Slomka
Submarine Explorer – A low cost AUV
The demonstrator is a low cost autonomous underwater robot. The computer system controlling the robot is design using advanced hardware/software codesign techniques by using state of the art FPGA SOPC technology implementing time critical parts of the system in hardware.

University of Bremen, Christian Genz See Day 1
A graphical SystemC refinement tool

University of Tokyo, Yoshihisa KOJIMA
A verification environment for high-level designs based on system dependence graphs
This tool provides a verification environment for high-level design descriptions. Program slicing, static code checking, dynamic simulation and formal equivalence checking based on symbolic simulation are realized on top of our ExSDGs.

University of Newcastle upon Tyne, Andrey Mokhov
Workcraft: a static data flow structure editing, visualisation and analysis tool
Reliable high-level modelling constructs are crucial to the design of efficient asynchronous circuits. The tool offers a GUI-based framework for visual editing, simulation, animation and extendable analysis features for different SDFS types.

14:00 – 16:00

University of Tehran, Mahshid Sedghi See Day 1
TLM Synthesis Studio

Osaka University, Ittetsu Taniguchi
SoC Architecture Explorer
Architecture design in IP-based design is difficult because of vast design space. SoC Architecture Explorer explores the design space automatically and a number of architectures are output, which have a trade-off relation between performance and hardware area.

14:00 – 16:00 SoC, Platforms and SystemC

Université de Bretagne Sud, Johann Laurent See Day 1
SoftExplorer

Université de Bretagne Sud, Rachid Dafali
µSPIDER CAD TOOL: CASE STUDY OF NOC IP GENERATION FOR FPGA
This demo presents the µSpider CAD tool for network on chip design under latency and bandwidth constraints and described the different steps of the associated design flow.

Eindhoven University of Technology, Sander Stuijk See Day 3
SDF3

University of Bonn, Andreas Raabe
A Reconfiguration Simulation Library For SystemC
This demonstration presents a library for modelling reconfiguration in SystemC combining IP reuse and high-level modelling with reconfiguration. Control statements and techniques that allow safe process controlling in conjunction with SystemC constructs are presented. A case study proves its applicability.

Chemnitz University of Technology, Uwe Proß
Specification data gathering
The Software gathers information about the system and its behavior on specification level and will check this specification for consistency. It enables Reuse of testcases as well as requirements and cost engineering.

Universität Karlsruhe, Jürgen Becker
MORPHEUS integrated toolset
The toolset compiles annotated c-code to ARM binaries while replacing the annotated function calls with calls the equivalent configurations on one of the heterogeneous reconfigurable engines of the MORPHEUS SoC.

16:00 – 18:00 Hardware Solutions

Université de Bretagne Sud, Philippe Coussy See Day 3
GAUT – A High-Level Synthesis tool for DSP applications

Université de Bretagne Sud, Pierre Bomel See Day 3
A lightweight and remote partially reconfigurable platform

Université de Bretagne Sud, Pierre Bomel See Day 3
A mixed (hardware and software) rapid prototyping platform.

Eindhoven University of Technology, Andreas Hansson See Day 3
CoMPSoC - A Composable and Predictable Multi-Processor System-on-Chip Template

Universidad Complutense de Madrid, Francisco Vallejos See Day 3
OS based Wireless Body Area Network for ECG

University of Bonn, Stefan Hochgürtel See Day 3
A broadband FFT-Spectrometer at work

Technical University of Denmark, Jan Madsen
Formal Verification of Design Properties of Hardware Architectures
We present a formal language for hardware models based on the Gezel hardware description language developed and maintained by Virginia Tech, USA. We show how the language can be used in connection with verification by relating the semantical domain to timed-automata using the UPPAAL system.

University of Rostock, Peter Danielis
Trust-by-Wire in Packet-switched IP Networks: Calling Line Identification Presentation for IP
The packet processing system IPclip (IP Calling Line Identification Presentation) is presented. It is implemented on an FPGA board and configurable at runtime via a graphical configuration tool. The functionality is demonstrated in a localization scenario using an analysis tool and Google Earth.

3 Thursday March 13, 2008

10:00 – 12:00 System Exploration with Software and Hardware	
Eindhoven University of Technology	CoMPSoC
	SDF3
University of Bonn	FFTS
University of Paderborn	Hardware-in-the-Loop Simulations
	General Purpose VLIW Processor
Politecnico di Milano	STShell
TU München	TaillightEngine

12:00 – 14:00 High Level Synthesis	
RWTH Aachen University	MPSoC Exploration Technique
University of Limerick	Data Converter BIST Solutions
University of Bremen	SC_refine
University of Tehran	TLM Synthesis Studio
Université de Bretagne	GAUT
Norwegian University of Science and Technology	Power-efficient parallel multipliers
University of Tehran	UT-TLM

14:00 – 16:00 Physical Design, Modelling and Exploration	
Université de Bretagne Sud	Lightweight
Université de Bretagne Sud	PALMYRE
Universidad Complutense de Madrid	Wireless Body Area Network
Technical University of Braunschweig	SYM TA/S
University of Tehran	SystemC Studio

10:00 – 12:00 System Exploration with Software and Hardware

Eindhoven University of Technology, Sander Stuijk
SDF3
The tool implements a state-of-the art design flow that can map a throughput-constrained application modeled with a Synchronous Dataflow Graph onto a NoC-based MP-SoC while providing timing guarantees. The design flow analyzes the resources requirements of the application, allocates the required resources in the NoC-based MP-SoC, and schedules accesses to shared resources.

University of Bonn, Stefan Hochgürtel
A broadband FFT-Spectrometer at work
We present a fully functional FFT-spectrometer card, calculating 2048 channels at a bandwidth of up to 1500 Mhz. Multiple parameters as well as the complete spectrometer-core can be altered at run-time over ethernet.

Eindhoven University of Technology, Andreas Hansson
CoMPSoC - A Composable and Predictable Multi-Processor System-on-Chip Template
We propose a Composable and Predictable Multi-Processor System-on-Chip platform and mapping methodology. Multiple real-time jobs can run simultaneously. Incremental integration and platform virtualisation are supported.

University of Paderborn, Christopher Pohl
Hardware-in-the-Loop Simulations with Matlab/Simulink/ModelSim for FPGA based designflows
This demonstrator shows the design flow and a working example of our Hardware-in-the-Loop Design Environment for FPGAs. Arbitrary VHDL designs can be automatically integrated into simulation or visualization tools, enabling functional verification and real time monitoring of that hardware design.

University of Paderborn, Thorsten Jungeblut
General Purpose VLIW Processor for Multiband-Multistandard applications
This demonstrator proposes our General Purpose VLIW-Processor for applications on mobile phones. Four arithmetic logical units can process scalar or SIMD instructions in parallel. The system is designed for 300 Mhz and achieves a performance of 1.2 GIPS or 2.4 VOPS.

Politecnico di Milano, Vittorio Zaccaria
System Tuning Shell: A Design Space Exploration Tool
System Tuning Shell is a design space exploration tool for supporting platform-based design. The tool allows users to plug-in custom system models and apply several optimization strategies to derive trade-offs on the system cost functions.

TU München, Christopher Claus
Hardware/software architecture of an algorithm for vision-based real-time vehicle detection in dark environments
The demonstrator runs on an ML310 board from Xilinx. Images are loaded from the connected hard drive into the main memory (DDR SDRAM) which is located on the board. From there, the pixel data can be accessed by a hardware coprocessor called TaillightEngine which is able to detect cars in dark environments.

12:00 – 14:00 High Level Synthesis

RWTH Aachen University, Torsten Kempf
An ESL Workbench for early MPSoC Design Space Exploration
One major issue in future MPSoC designs is the combined HW and SW development, often referred to HW/SW co-design. Here, both HW and SW are developed in parallel manner, imposing new design challenges to the system architects. To cope with this issue during MPSoC design we have proposed a higher abstraction level, where an abstract processor simulator called Virtual Processing Unit (VPU) is utilized.

University of Limerick, Ian Grout
CMOS Implementation for Data Converter BIST/BOST
Two silicon implementations for BIST and BOST solutions for data converter self-test are to be demonstrated. In these solutions, self-test functions for 16-18 bit data converter designs are undertaken with communications to an external PC. The systems provide the capability for on-chip or on-DIB signal generation, data capture and communications.

University of Bremen, Christian Genz See Day 1
A graphical SystemC refinement tool

University of Tehran, Mahshid Sedghi See Day 1
TLM Synthesis Studio

Université de Bretagne Sud, Philippe Coussy
GAUT – A High-Level Synthesis tool for DSP applications
Starting from a pure C function GAUT generates a potentially pipelined architecture composed of a processing unit, a memory unit, a communication unit with a GALS/LIS interface. The synthesis constraints are the data average throughput, the clock frequency, the FPGA/ASIC target technology and optionally the memory architecture/mapping, the I/O timing diagram. GAUT generates VHDL and test benches which are inputs for commercial logical synthesis tools.

Norwegian University of Science and Technology, Saeeid Tahmasbi Oskuii
Low Power Partial-Product Reduction-Tree Generator for Parallel Multipliers
A method will be presented to generate of power-efficient parallel multipliers to minimize activity. At each stage of the reduction tree, a simulated annealing optimizer uses power cost numbers from a specially implemented probabilistic gate-level power estimator and selects a power-efficient solution.

University of Tehran, Parisa Razaghi
A Platform for Multi-Language Mixed-Signal Simulation
Mixed-Signal Simulator is a mixed-signal, mixed-domain, and mixed-language design environment which supports VHDL-AMS 1999, VHDL-2002, Verilog 2001, SystemVerilog 2005 assertions, and SystemC 2005.

14:00 – 16:00 Physical Design, Modelling and Exploration

Université de Bretagne Sud, Pierre Bomel
A lightweight and remote partially reconfigurable platform
We present the concept of a networked lightweight and partially reconfigurable platform assisted by a remote bitstreams server. We propose a software and hardware architecture as well as a new data-link level network protocol implementation dedicated to dynamic and partial reconfiguration of FPGAs.

Universidad Complutense de Madrid, Francisco Vallejos
OS based Wireless Body Area Network for ECG
We present a complete architecture of a Wireless Body Area Network for ECG monitoring. The network is composed of five nodes and a base station. The nodes proccess the ECG signal that they sense and they send information to the base station when a special event occurs, depending on the application. We have developed a new TDMA protocol that reduces the energy consumption associated with the radio.

Université de Bretagne Sud, Pierre Bomel
A mixed (hardware and software) rapid prototyping platform.
PALMYRE is set of hardware components and software tools enabling the rapid prototyping of telecom-oriented application. DSPs from Texas Instruments and FPGAs from Xilinx can be freely mixed to build a specific computing and communication topology. The demonstration is a pipeline of two DSPs and an FPGA Viterbi decoder.

Technical University of Braunschweig, Steffen Stein
Advances in Symbolic Performance Analysis
We will demonstrate the latest advances in formal performance analysis and its application for runtime performance control. We will demonstrate approaches to embedded performance control, current research in event stream modeling and analysis approaches applicable for MPSoC.

University of Tehran, Homa Alemzadeh
SystemC Studio: Translation for TLM Combined Simulation and Synthesis
SystemC Studio provides an interface between RT level VHDL/Verilog descriptions and high level descriptions in SystemC and SystemC TLM. This environment also provides SystemC translation to VHDL for RTL synthesis of post high-level synthesis TLM descriptions.