

News & Analysis

Consortium completes VSIA QIP Metric Beta Program

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SAN FRANCISCO — The Virtual Socket Interface Alliance (VSIA) said Tuesday (Dec. 13) that Semiconductor Technology Academic Research Center (STARC), a Japanese research consortium, was among the first organizations to complete the VSIA QIP Metric Beta Testing Program.

Beta test was executed by the intellectual property (IP) quality working group in STARC, according to [VSIA](#) (Wakefield, Mass.)

The [VSIA QIP](#) (quality intellectual property) Metric Beta program, established in August, attempts solve the growing problem of IP integrations by bringing measurability to assessing the quality of an IP core from a vendor by assigning a quality score that captures various metrics including vendor capability, design practices, and IP core documentation and deliverables.

In addition to [STARC](#), companies participating in Beta testing of the QIP Metric include Cadence Design Systems Inc., Denali Software Inc., edacentrum, Freescale Semiconductor Inc., LSI Logic Corp., Mentor Graphics Corp., Philips, STMicroelectronics and others, VSIA said. The QIP Metric is expected to be released to the public in the first quarter of 2006.

“VSIA has always seen Japan as an important player in the world semiconductor arena. The Japanese special interest group was our first regional SIG,” said Mike Kaskowitz, VSIA president, in a statement. “Participating in the VSIA QIP Metric Beta and being among the first to complete the program show STARC’s desire to influence international standards.”

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