SWOT Analysis of the Technology Design Ecosystem

3rd NANO-TEC Workshop took place in Lausanne, Switzerland on May 30–31, 2012

The project NANO-TEC ("ECOSYSTEMS TECHNOLOGY and DESIGN for NANOELECTRONICS") organizes a series of workshops in order to establish a joint Design-Technology Community for Nanoelectronics in Europe. During the 1st NANO-TEC workshop in January 2011 the requirements for future 'Beyond CMOS' devices have been identified. These devices have been benchmarked during the 2nd workshop in October 2011. The objective of the 3rd workshop in May 2012 was to conduct an analysis on the strength, weaknesses, opportunities and threats (SWOT analysis) of the benchmarked devices. This analysis took into account the technology and design aspects, but also application perspectives. The target outcome of the workshop was a number of exploitation scenarios for selected number of 'Beyond CMOS' devices. As the detailed documentation of the workshop is currently set up, this article gives only a short overview on the workshop. Additionally it provides a report of the panel session, which took place at the end of the workshop.

Workshop Overview

As both previous workshops, also the 3rd workshop comprises several sessions with plenary presentations followed by a discussion on 'Beyond CMOS: from Technology to Applications'. Each session addressed a SWOT analysis of the specific 'Beyond CMOS' device technology, including the required scientific and technical capabilities, application perspective, and infrastructural considerations and gave a clue on possible exploitation scenarios for these devices. The following presentations have been performed:

Prof. Dr. Sense Jan van der Molen, Leiden University
Molecular Electronics

Dr. Heike Riel, IBM Zurich
Nanowires

Prof. Dr. Charles Gould, University of Wuerzburg
Spintronics

Dr. Michael Gaitan, NIST, Gaithensburg, MD, U.S.A.
MEMS

Prof. Dr. Max Lemme, KTH Royal Institute of Technology, Stockholm
Graphene

Goran Wendin, Chalmers University of Technology, Gothenburg
Solid-state Quantum Computing

Dr. Julie Grollier, CNRS-Thales, Palaiseau
Neuromorphic Computing

Panel Discussion, Chair: Dr. Livio Baldi, Micron Technology Inc., Milan

"Beyond CMOS: from Technology to Applications"

As final part of the workshop programme, Livio Baldi (Micron Semiconductors, Italia) chaired a panel entitled "Beyond CMOS: from Technology to Applications". The panelists were the professors Wolfgang Rosenstiel (edacentrum and University of Tübingen, Germany), Paolo Lugli (Technical University of Munich, Germany), Giovanni de Micheli (École Politechnique Fédérale de Lausanne, Switzerland) and Sandip Tiwari (Cornell University, Ithaca, N.Y., USA).

Funding Label:
ICT-2010-257964

Runtime:
09/01/2010 – 02/28/2013

Homepage:
www.fp7-nanotec.eu

The slides of all the presentations can be found at https://www.fp7-nanotec.eu/workshop3/presentations

Abbildung 3.31: More than 50 participants joined the 3rd NANO-TEC-Workshop in Lausanne

Abbildung 3.32: Livio Baldi, Micron Technology Inc., Milan

In the beginning, Livio introduced the discussion reminding that it took 50 years and a few hundred billion dollars to go from a few transistors to the present complexity and that despite this effort design is still a limiting factor in CMOS integration density. With this background and looking at the new beyond CMOS technologies he formulated several questions to be answered by the panelists and during the discussion:

- What can a new (beyond CMOS) technology do to improve the situation of CMOS and who is going to pay for it?
- Which types of applications will be the drivers for 'Beyond CMOS'?
- Will they all compete for the same killing application, or will they share the market?
- Will design challenges be different for different applications?
- Can design tools be the discriminating factor for the success of one specific technology?
- Present design tools are a huge legacy: what can trigger the investment needed for new tools?

Afterwards the panelists took the opportunity to give their point of view on the situation.

Prof. Dr. Sandip Tiwari, Cornell University, Ithaca, N.Y.
Sandip was first stating, that design as a limitation in CMOS integration density is a self-inflicted wound. This is because of the steadily growing complexity met only by the introduction of hierarchy and because of the growing number of constraints (i. e. due to energy consumption). As these aspects have not been considered during the creation of the CMOS design process itself a now "creeky infrastructure" has been developed which is hardly able to cover today's CMOS design problems. Therefore Sandip demands for a stronger foundation of the design at system level, in order to be able to stand the design challenges using new technologies.

With respect to the possible drivers for 'Beyond CMOS', Sandip mentioned ultra-low power Microsystems, machines with learning or inference capabilities and effective education platforms. Sandip agreed that design challenges will be different for different applications although he also sees common aspects. As Apple now is successful with good design Sandip is convinced that design tools can be the discriminating factor for the success of one specific technology because a design tool is the codification of a design process and its mathematical translation which itself makes the difference. Additionally Sandip named the energy challenge and the application challenge due to the changing society as triggers of the investment in new tools that could break the huge legacy of present design tools.

Finally, like in the previous NANO-TEC workshop, Sandip demands for a new open infrastructure that brings people and things together. He characterizes this as an international-national scale problem that crosses frontiers of many disciplines, that needs a cooperative effort with much thinking at its start and long project duration under a unified leadership.

Prof. Dr. Wolfgang Rosenstiel, edacentrum and University of Tübingen
Wolfgang introduced his position with a characterization of design stating that every circuit being designed today, starts with a computational model at a high level of abstraction, then goes through a sequence of synthesis and optimization transformations, followed by rigorous digital simulation and prototyping, as well as formal and semi-formal verification, before it is finally manufactured via advanced lithographical and chemical processes.

In order to be able to design efficiently, an automation process (Electronic Design Automation) has been established. This came out of one of the earliest inter-disciplinary collaborations: Computer scientists and engineers in EDA collaborated successfully with the electrical engineers to derive various levels of circuit models, physicists and chemists worked together to find manufacturing models, theoretical computer scientists conducted various kinds of complexity analyses

newsletter edacentrum - Sample

Order the complete article
at newsletter@edacentrum.de

edacentrum, Hannover, August 2012

Abbildung 3.33: Sandip Tiwari, Cornell University, Ithaca, N.Y.

Abbildung 3.34: Wolfgang Rosenstiel, edacentrum and University of Tübingen