NANO-TEC: Ecosystems Technology and Design for Nano-electronics

Coordination Action (CA) within the FP7 ICT Work program shows first results, but there are still things to be done ...

Especially in the Beyond CMOS area the interaction between the research communities of design and technology is characterized by a diversity of terminologies, modes of operation and the absence of a consensus on main priorities. Therefore the NANO-TEC project aims to bring together these communities for the benefit of a stronger European Research Area in future. To achieve this goal the project organizes a series of four workshops to elaborate their findings from identification over benchmarking and an analysis on the strengths, weaknesses, opportunities and threats (SWOT analysis) up to recommendations. These workshops are flanked by a website with different networking functions to stimulate and support the scientific exchange, in particular on the workshops content and results.

This article contains an introduction to the EU project NANO-TEC and its findings up to the third workshop on SWOT analysis, which meanwhile took place in the end of May in Lausanne, Switzerland. It includes a summary of the – for the NANO-TEC project – most promising technology trends. Further on it shows a preliminary benchmarking analysis for some of these trends as an example of the project work. Additionally relevant design issues concerning these technologies are summarised followed by conclusions and recommendations to bridge this design-technology gap..

Introduction

As scaling CMOS technology already longs for nearly 50 years, many experts expect that it is coming to an end in the next decades. And the arising questions are: what will come after CMOS? What kind of technology could be used instead? Will Europe play an important role in Beyond CMOS technologies and thus have a significant market share with jobs using emerging technologies? And if not, what will happen to European industries in sectors such as the automotive and energy ones, which heavily depend on electronic system competences?

In industrial R&D design and technology go hand in hand to achieve an imminent generation of devices and systems. However, for future generations in nanoelectronics, design and technology are not sufficiently integrated to ensure a fast exploitation in the form of products. The capability of Europe to transfer and exploit research results in nanoelectronics depends on the availability of integrated solutions provided by a joint design and technology community.

About NANO-TEC

To this end, a coordination action (CA) within FP7 ICT Work program from Call 5 has been started in September 2010. It is called "Ecosystems Technology and Design for Nanoelectronics" (NANO-TEC) and it has two main objectives:

- Identify the next generation of (emerging) device concepts and technologies for ICT.
- Build a community of academic researchers in nanoelectronics, addressing specifically research in Beyond CMOS from the combined technology and design perspectives.

The NANO-TEC CONCEPT

Within the project NANO-TEC, the relationship between technology and design in nanoelectronics is seen as a mutually dependent two-block partnership (Figure 1.01). Consider a function of relevance to Beyond CMOS, which comes out of the myriad of possibilities arising from the fast progress in material sciences, coupled to developments in the control of morphology and the nanostructuring of these materials. A crucial next step is to find a way to link this function to an established, or a new, logic. For this logic to work, ideas on design and architecture are needed. In this basic frame of analysis, design plays a key enabling role in the latter two steps, as well as in the consideration of the way the information-related function, based on of these new materials and (nano) structures, is linked to a logic system

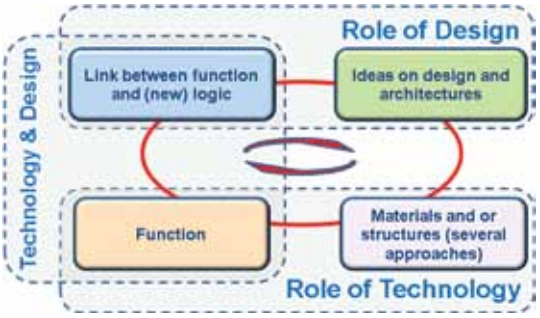

Figure 1.01: The NANO-TEC project concept

Methodology of NANO-TEC

A methodology for continued consultation and analysis of research needs and trends is carried out by NANO-TEC. Two elements are crucial here.

Funding Label:
ICT-2010-257964

Runtime:
09/01/2010 – 02/28/2013

Homepage:
www.fp7-nanotec.eu

The NANO-TEC Workshop Series

One is the access to the huge expertise in Europe, albeit still fragmented, in the area of Beyond CMOS both in technology and in design. This is carried out by a workshop series with invited international experts, mainly from Europe and some from the Americas and Asia. These workshops are preceded by a methodology-contents preparation phase and subsequent analysis and documentation, both by the consortium. Apart of determining what is relevant for Beyond CMOS devices and design, benchmarking and SWOT analyses will be performed within these workshops. The first workshop tried to identify emerging nanoelectronic technologies and the designs for new devices to work. These are discussed in section on technology trends in Beyond CMOS below. The 2nd Workshop focused on benchmarking of these and a few more emerging technologies and the preliminary outcome is presented in the section on examples of benchmarking. The 3rd workshop in this series, on the SWOT analysis, has taken place in May 2012 (s. page 35) and its results will be publicly available shortly. An end-of-the-project public dissemination event on November 5–6, 2012 in Barcelona will present the results of the work of NANO-TEC to stake-holders, including the EC and relevant ETPs.

The presentations of all workshops and their documentation is available at https://www.fp7-nanotec.eu/events/

The sessions of all workshops follow a certain fixed pattern: They have an invited speaker, a "discussant", to stimulate a discussion on the session's topic and a "rapporteur" to take over the documentation. During the second workshop a working group per topic has been established, which discussed in more detail the topic's benchmarking aspects. Each workshop had a Panel discussion focusing on design issues and the bridge to technology. Each workshop had about 70researchers attending. Participation has been open to all EU ICT project coordinators and partners as well as to the nanoelectronics community in Europe, e.g. ENIAC Scientific Community Council, SINANO Institute, ENI2 consortium partners, and the Design European Networks. The presentations of speakers, discussants and rapporteurs can be found at the above-mentioned project web site.

The Web-based Platform of NANO-TEC

The other crucial element is a web-based platform to carry out the work and document it. The web-based work platform is part of the long-term community-building aim and it enables an exchange of documents as well as web-based discussions. Furthermore the platform will provide the place where working groups can evolve into a Specialist Interest Group on the combined ecosystems of technology and design.

NANO-TEC invites all interested experts (especially those from the design side) to join the working group on the future of Beyond CMOS. Just contact Ralf Popp at popp@edacentrum.de.

Technology Trends in Beyond CMOS

The discussion on trends benefitted from an excellent overview on Nanoelectronics given by Jeffrey Welser (Semiconductor Research Council and IBM) coming from a series of global workshops held in 2010 organised by the National Science Foundation and the National Nanotechnology Initiative [1]. In particular, the USA Semiconductor Research Council and the Nanoelectronics Research Initiative have identified five research vectors:

- New devices: Devices with alternative state vector.
- New ways to connect devices: Non-charge data transfer.
- New methods for computation: non-equilibrium systems.
- New methods to manage heat: Nanoscale phonon engineering
- New methods of fabrication: Directed self-assembly.

The approach followed by NANO-TEC concentrates on specific emerging technologies, namely

Carbon-based Electronics

The unique and versatile physical properties of graphene, make it the preferred material in this group for future electronics and electronics-related applications. Devices already demonstrated include MOSFET with record mobility and transconductance as well as THz devices. Large area flexible electronic applications have also been demonstrated [2]. It is generally agreed that graphene will find several applications in the More than Moore area. The main issues with graphene were identified as (i) the need to engineer a stable and uniform non-zero gap graphene, i.e., bilayer graphene, (ii) its manufacturability and (iii) integration with existing Si-CMOS.

Silicon-based Electronics

This is the current dominant technology which upon further scaling faces lithography limits, short channel effects and thermal constraints, among others [3]. There is a strong need for new transistor architectures and for novel designs for interconnections since, it is argued, optical interconnects are unlikely to offer a viable solution in the short term. Physical limits are not yet reached. A key challenge is the economic one which is leading to an increasing outsourcing, with the associated negative impact in jobs in Europe and raising questions on the need for R&D, and perhaps training, in technology in Europe. This is, where the interaction technology-design is most urgently needed.

Compound Semiconductor-based Micro and Nanoelectronics

The trends in III-V semiconductor compounds were identified as [4]: (i) Scaling of dimensions to 10's of nm, along with development of new materials for contacts, dielectrics, etc. along with new processes for III-V HBTs and HFETs. There are a variety of III-V heterostructure material choices and variations in device physics employed. (ii) Compound SC integration in silicon technologies. Two examples: Incorporation of III-V materials synergistically with Si for higher speed n-channel and p-channel MOSFETs, i.e. getting the III-V on the Si and, InGaAs MOSFET with 3.5 nm channel on a semi-insulating substrate wafer bonded to

Si. (iii) Interest on III-V nanotechnologies (nanowires) such as vertical wrap-gated nanowire transistors. However, the question of single transistor fabrication from each nanowire and interconnection of nanodevices into ICs is still open. The main advantage of integrating III-V semiconductors with Si technology is band gap engineering.

Spintronics and Magneto Electronics

Fundamental phenomena associated with giant magnetoresistance, tunnel magnetoresistance and devices for MRAM (Magneto-resistive Random Access Memory) are understood and are based on the dependence of transmission spin currents depending on the orientation relation of adjacent ferromagnetic layers. In contrast to systems that are based on charge transport, spin dynamics opens the possibility for non-volatile low dissipation memory devices, since charges do not need to be in motion for information transport. magnetoresistive devices for magnetic sensing and for data storage have already been commercialized. Currently, pure spin currents without charge transfer in integrated circuits are controlled by magnetic fields or spin-polarized charge currents. In the future they might be controlled by electric fields. Intriguing new physical discoveries from which practical possibilities could emerge are for instance RF-applications, spin logics, the spin-Hall effect, the spin-Seebeck effect and quantum computing. The recent advent of topological insulators, which carry non-dissipative spin currents, could lead to a paradigm change [5]. At present, real possible applications utilizing these new discoveries are sometime still unclear. Mayor challenges include: reliability and stability issues, electrical contacts (interfaces) and interconnects. The latter could be minimized by multifunctional devices and, although some basic concepts are already developed, support for device structure design and for developing disruptive new architectures is needed.

Molecular Electronics

Molecular electronic devices can be divided in three categories based on size of the device: i) single molecule electronics, ii) self-assembled molecular electronics and iii) thin-film molecular electronics. The single molecule devices represent a very long term approach and much work is needed to gain insight into the behaviour of the molecules, not to mention optimising the properties for data handling and integration [6]. Some of the thin-film molecular electronic devices are already in commercial production, including OFETs, OLEDs and displays. For the next generation Beyond CMOS devices self-assembled molecular electronics is a potential candidate. Reasonable gain and low power consumption have been demonstrated with devices in which self-assembling monolayers replace gate dielectrics, making integration possible [7, 8]. Also, the recent progress in neuron inspired devices is promising [9]. Fabrication can be solution based and on flexible substrates. Drawbacks are slow speed and, when using the molecules as active part of the device, the still poor understanding of the behaviour of the molecules.

Solid State Quantum Computing

The potential of quantum computing has been recognised for a long time but the real implementation is still missing due to issues related to de-coherence limited computing time and difficulties in integration [10–12]. Quantum computing relies on the coupling of switching quantum bits, or qubits, and one of the advantages of quantum computing is that it consumes no energy at the qubit level. Currently, Josephson junction qubits seem to provide the most promising way to integration and realisation of computers with high number of qubits [13]. This technology is also compatible with Si CMOS processing. Although it is still long way in the future, with 100 integrated qubits a quantum computer would surpass in the efficiency any foreseen classical supercomputer with much smaller power consumption. The drawback is that a quantum computer can solve a limited number of problems and only a few algorithms are available. Also, with increasing number of qubits error correction may consume a major part of the computational resources.

MEMS

In MEMS/NEMS almost all the domains of physics are present. They are new technologies that can have a strong impact on normal life and nowadays they have yet to bet completely accepted by the users [14]. MEMS/NEMS are rather complex while simultaneously they must be reliable and low power. In fact they must incorporate autonomous management of power.

The current technology trends are: the merging of top down and bottom up approaches, MEMS/NEMS with functional multi-layers suitable for heterogeneous integration, and increasing system approach, increasing number of applications in harsh environments requiring SiC-, Diamond- and Graphene- based MEMS/NEMS, biocompatibility and flexibility.

Among the most important challenges for MEMS technologies, the following can be included: (i) Miniaturization related to size matters requiring that the design tools and simulation programs must be upgraded to the new solutions. (ii) For integration the most important point is to manage complexity. Monolithic vs. heterogeneous solutions must be considered as performances vs. both, costs and volume. Integration is a key point, because the “user” wants a system. (iii) MEMS/NEMS must be autonomous, with a long life.

newsletter edacentrum - Sample

Order the complete article
at newsletter@edacentrum.de

edacentrum, Hannover, August 2012