Nachrichten von den Projekten

VeronA is going to present recent results in a special session at DATE'09

For a speed-up of analog design cycles to keep up with the continuously decreasing time to market, iterative design refinement and redesigns are more than ever regarded as showstoppers. To deal with this issue, referred to as design and verification gap, the development of a continuous and consistent verification is mandatory. In digital design, formal verification methods are considered as a key technology for efficient design flows. However, industrial availability of formal methods for analog circuit verification is still negligible despite a growing need.

The panel discussion „Formal Approaches to Analog Verification – Now or Never?" takes place on Wednesday, April 22, 2009 from 11.00 to 12.30. Location is the Exhibition Theatre at DATE'09.

Within the VeronA project, research institutions have made considerable advances in the area of formal verification of analog circuits. Therefore, they have organized a special session entitled "Formal Approaches to Analog Verification – Now or Never?" where they will present and discuss a selection of four recent approaches in analog verification that cover a broad scope of verification philosophies:

- Approach 1 comprises a classical simulation method, challenged by the integration of circuit models and simulators of different modes and domains.
- The approaches 2 and 3 deal with formal methods considering manufacturing tolerances and operating variations. Both are based on the formulation of circuit performances derived from the classical domain of nodal circuit analysis.
- Approach 4 considers formal verification of analog circuits based on circuit properties that are derived from an entire coverage of the state space.

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The first part of this session comprises a tutorial, where these approaches will be explained. The second part is a discussion with additional participants from industry. It will be about the maturity of formal approaches to analog verification and will cover whether they are ready for practical application now (... or never?), which parts are still missing, and if it will ever reach the stage of formal verification for digital circuits.

Kont@kt (RapidMPSoC)
Andreas Foglar
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Presenters:

- 1. Yifan Wang, RWTH Aachen, Chair of Integrated Analog Circuits, Germany
- 2. Markus Olbrich, University of Hannover, Institute for Microelectronic Systems, Germany
- 3. Helmut Gräb, Technical University of Munich, Institute for EDA, Germany
- 4. Sebastian Steinhorst, University of Frankfurt, Institute for Computer Science, Germany

Directly after the panel discussion some of the VeronA project partners are available for a personal contact at the edacentrum booth (EP9). They look forward to your visit. (Pp)

RapidMPSoC: Infineon holt Chip-Entwicklung zurück nach Europa

Dank der Ergebnisse des Förderprojektes RapidMPSoC im ersten Projektjahr konnte die Entwicklung für einen neuen Chip aus Asien zurück nach Europa (München

Newsletter edacentrum Probeauszug

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