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Low Power Design

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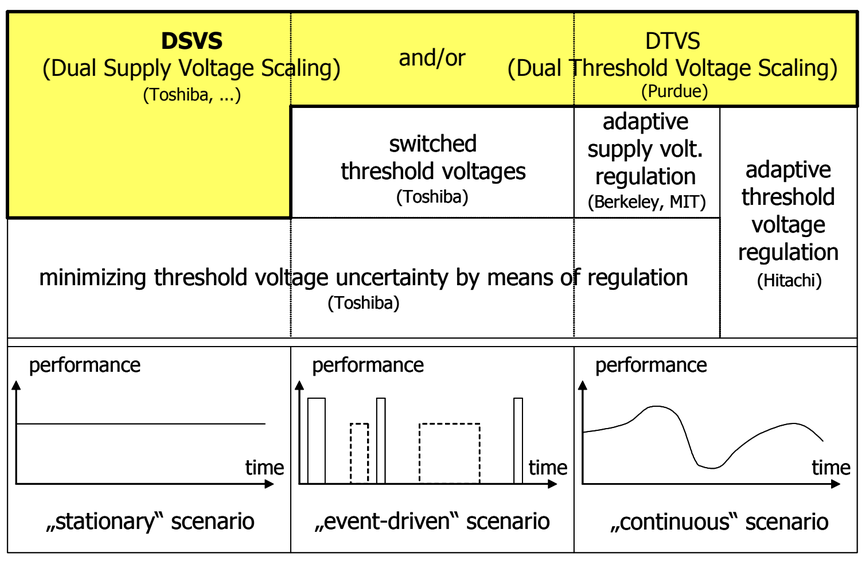
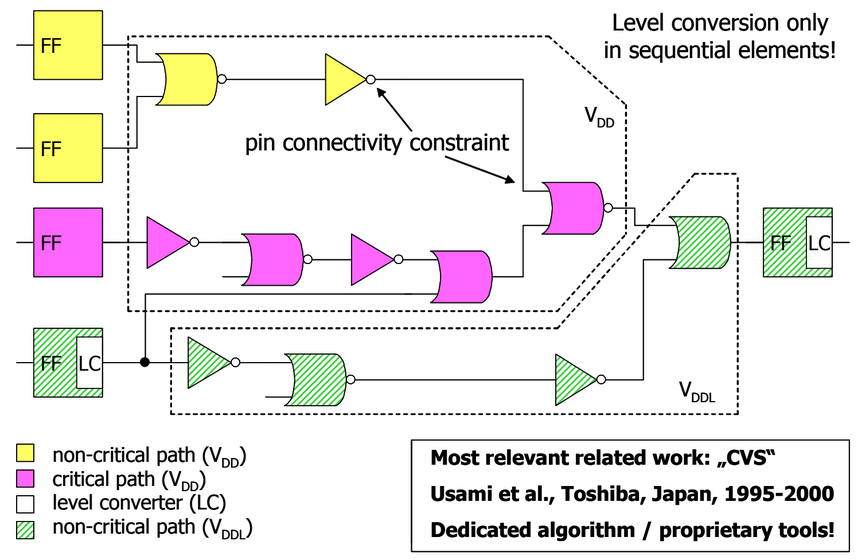
Advanced Voltage Scaling Techniques



Dual Supply Voltage Scaling (DSVS)



Most relevant related work: „CVS"
Usami et al., Toshiba, Japan, 1995-2000
Dedicated algorithm / proprietary tools!

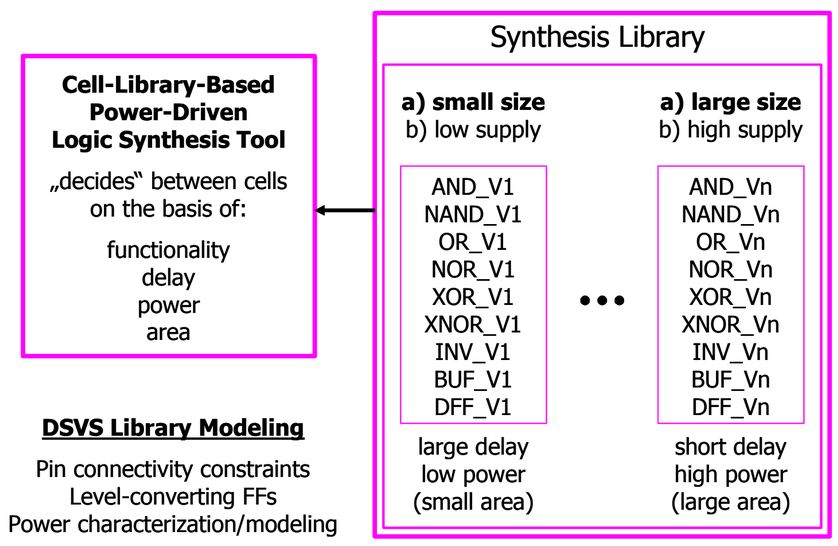
Sequential Benchmark Circuits

	Power red. SSV pwr. opt.	Power red. DSVS	Impact of DSVS on area
mm4a	25%	6%	+8%
mm9a	28%	11%	+6%
mm30a	23%	6%	+11%
mult32a	2%	24%	+8%
S713	32%	7%	-1%
S820	16%	10%	-5%
s1196	31%	5%	+6%
s5378	24%	10%	+21%
s9234.1	13%	8%	+15%
s38417	12%	17%	+28%
∅	21%	10%	+10%

Combinational Benchmark Circuits

	Power reduction due to		
	SSV pwr. opt.	DSVS	CVS
apex6	26%	10%	8%
c432	26%	3%	0%
c880	22%	12%	4%
c1908	30%	7%	6%
c3540	25%	5%	1%
c5315	23%	12%	9%
c6288	20%	6%	2%
c7552	17%	9%	5%
i10	28%	14%	11%
i5	28%	5%	5%
my_adder	24%	13%	6%
pair	26%	9%	8%
rot	28%	13%	10%
x3	28%	20%	11%
x4	35%	12%	9%
∅	26%	10%	6%

Exploiting Gate Sizing Tools for DSVS



Summary

- Modified conventional methodology:
  - Gate Sizing algorithm / tool
  - DSVS library
- Improvement over Single Supply Voltage power optimization:
  - Circuit-dependent: 3% - 24%
  - Average: 10%
- Clock voltage scaling is also supported!
- Application for $V_{threshold}$ scaling

From Ph.D. Thesis by Dr.-Ing. Torsten Mahnke:
„Low Power CMOS ASIC Design Using Voltage Scaling in the Logic Synthesis"
in cooperation with National Semiconductor