TECHNISCHE UNIVERSITÄT MÜNCHEN

Lehrstuhl für Integrierte Systeme

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Video Processing

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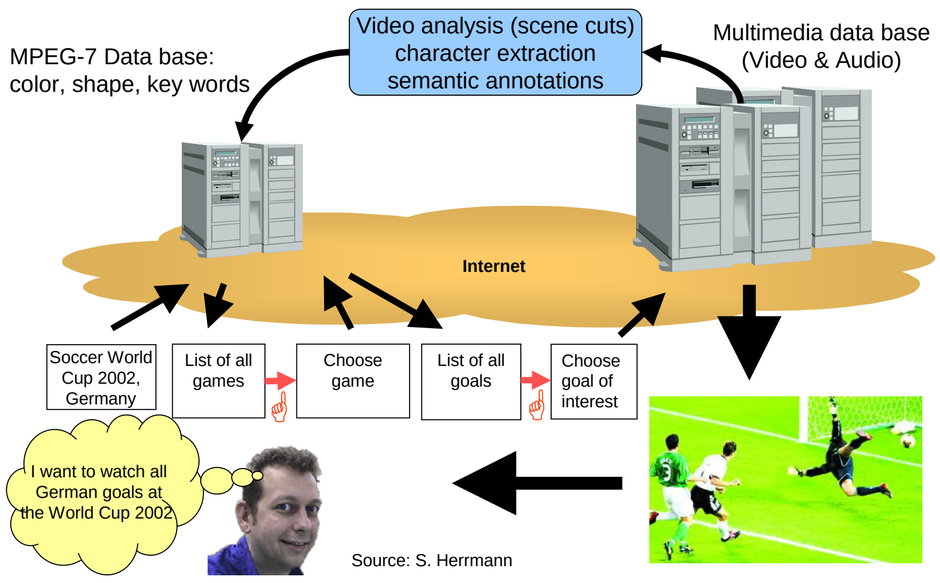
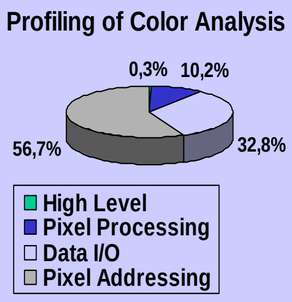
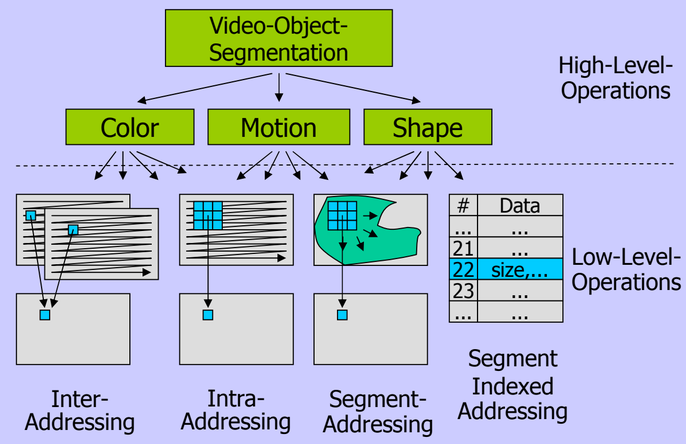
MPEG-7 Indexing and Retrieval



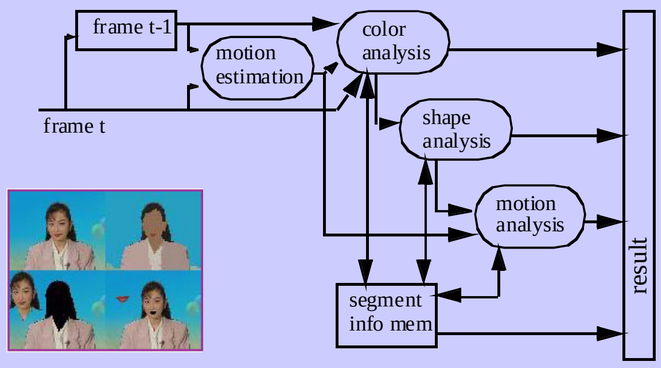
Video Object Segmentation

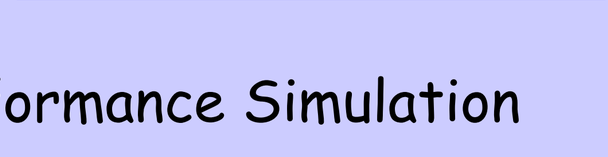
Where is CPU processing power burned?





Structure of Segmentation Algorithm





Dedicated HW Address Engine

- Area

Unit	[mm²]
Processing Unit [1]	1.8
Address Unit [1]	2.5
Add'l Logic [2]	0.6
Interconnects [2]	5.1
Cache Memory [3] (122 kByte)	18.1
Coordinates Memory (164 kByte) [3]	19.6
Total	47.7

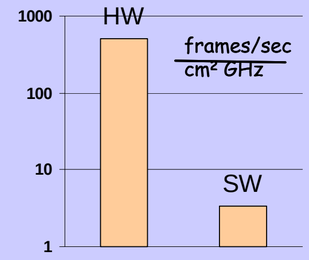
Techn.: ST/HCMOS7 0.25µm

- Processing Speed

Algorithm	
Watershed [4]	8.56 ms
Gradient [4]	2.03 ms
Erosion/Dilation [4]	1.52 ms
Relaxation [4]	3.60 ms
Iterative Color Segmentation [5]	49.2 f/s

Clock Frequency: 200MHz

- Cost Metric:



Cost Metric = throughput per Si Area per clock frequ.

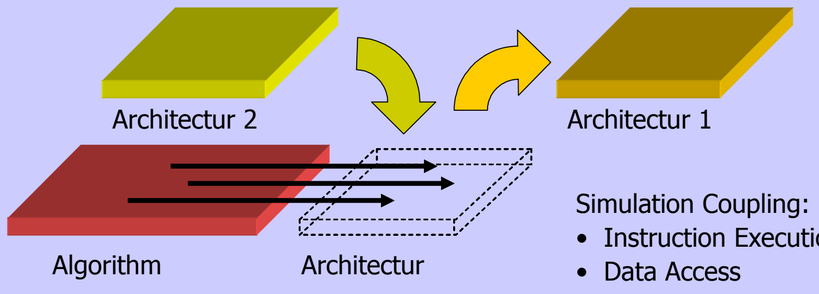
CIF = Common Interchange Format (352x288)
f/s = frames/sec, QCIF = Quarter CIF (176x144)

1) Synthesis Result
2) Estimation
3) Generated by RAM Compiler
4) Resolution CIF, YUV Color
5) Resolution QCIF, YUV Color

Performance Simulation

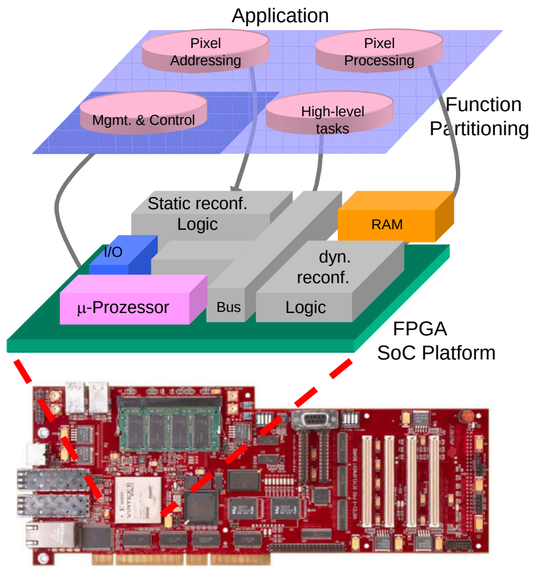
Function: $C = A + B$
Timing: $t_C = \max(t_A, t_B) + t_{add}$

Model Partitioning:
- Algorithmic Model: Software Model, functional
- Architectural Model: Timing and architectural effects



Simulation Coupling:
- Instruction Execution
- Data Access

The Next Steps: Reconfigurable Architecture



Hardware:
- Dedicated:
  embedded RISC, memory/ctrl, bus/ctrl, config/ctrl
- Static reconfig:
  Application-specific, e.g. pixel addr.
- Dyn. Reconfig:
  Changing operations within application, e.g. pixel processing

Software:
- Operation:
  Management of config. Data, monitoring & test, RTOS
- Application:
  High level operations, e.g. segmentation ctrl

European Projects: bu*man, KEHEMA

In cooperation with: Universitat Politècnica de València