Configurable System-on-Chip: Coarse-grain XPP-based Architecture Integration

LEON Microprocessor
- available as a free IP Core from ESA (European Space Agency)
- synthesizable VHDL model of a 32-bit processor with an instruction set according to the IEEE-1754
- LEON integer unit (IU) implements SPARC integer instructions as defined in SPARC Architecture Manual version 8
- 5-stage instruction pipeline

LEON Synthesis Results (2x8KB Caches)
- approx. 15,000 standard cells
- 0.9 mm² area requirements
- clock frequency up to 250 MHz

XPP64A Development Platform

CSoC - Components
- 8x8 XPP array
- Leon RISC microprocessor
- on-chip SRAM/ROM modules
- external memory controller
- multi-layer AHB Interconnect matrix
- IRQ-controller, UART, Timer, I/O ports

XPP - eXtreme Processing Platform
- Hierarchical array of coarse-grain Processing Array Elements (PAEs)
- powerful run-time reconfiguration mechanism
- main distinguishing features:
  - automatic packet-handling mechanism
  - sophisticated hierarchical Configuration protocols

XPP Application Results Example
- MPEG-4:
  - 3 different frame types
  - IDCT: 40 operations onto 4x4 XPP array
  - 74 clock cycles for decoding of a single 8x8 pixel block
  - PAL image:
    - 720x576 pixel x 24bit = 1.2 MB/frame
    - 25 frames/sec => 30 MB/s
    - 6480 blocks => 479,520 cycles/frame
    - 25 frames/s => 11,988,000 cycles/s

XPP Energy Consumption
- CMOS, 0.13µm, 100 MHz
  - Algorithm
    - MPEG Video 2D DCT (8x8)
    - Real 16 Tap FIR Filter (40 Samples)
    - 256-point FFT
  - XPP16
    - 19 nWattSeconds
    - 12 nWattSeconds
    - 515 nWattSeconds
  - DSP IP
    - 380 nWattSeconds
    - 453 nWattSeconds

Multi-layer AHB
- routes multiple transfers at the same time from masters to addressed slaves
- model is highly parametrizable with regards to AHB module count, AHB width, address spaces, etc.
- parallel transfers boost the maximum bus performance to a multiple of standard AHB performance