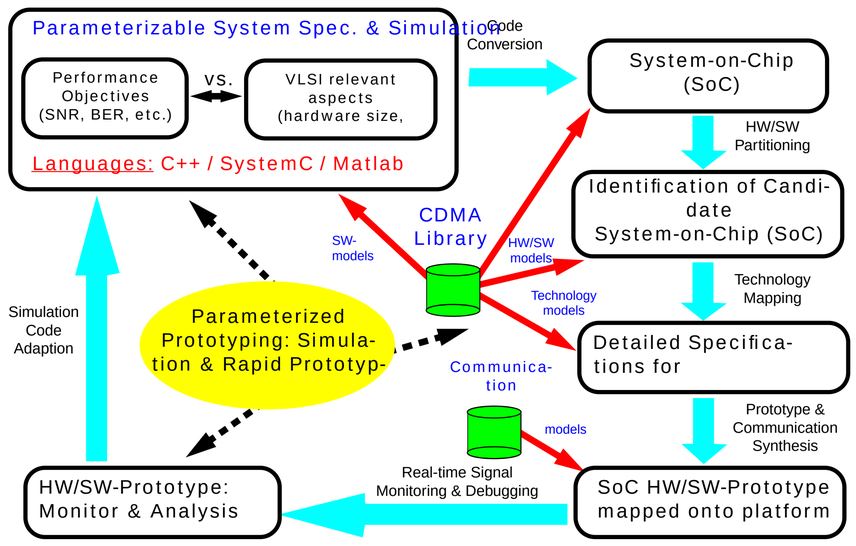
Advanced Design and Verification of ASICs (ADeVA)

IP-based EDA Project IP^2

IP^2: BMBF sponsored industry/academic research project



Goals:

Formal Spec + Simul./Prototyp. for flexible HW/SW Architectures
Automated Co-Synthesis into C- and synthesizable VHDL Models
Automated HW/SW Design Space Exploration:
Co-Design & Technology Selection

Application Specific:

Digital Baseband Processing in Mobile Communication

Specification

- Mostly textual
  - general requirements
  - register access
- control requirements
- System engineers & ASIC/SoC designers involved
- Common word processors (FrameMaker)
- Feature list linking via DOORS (requirement/document tracking system)
- Tracking using web based volume system
  - draft version
  - fixed, reviewed releases
- ASIC/SoC document (~300 pages, 1000 requirements)

100 REQUIREMENT BEGIN
Summary : mask register implementation
Application : system functional requirement
A mask register shall be implemented for every delta and event register in the device. The ending *E for event registers and *D for delta registers shall be replaced by *M for the generation of the mask register. The mask registers shall be 1 bit wide and shall have the type C-RW-control/mask.
Example: event register = BERTSFAILE; corresponding mask register = BERTSFAILM
REQUIREMENT END

170 REQUIREMENT BEGIN
Summary : Out-Of-Frame state declaration
Application : system functional requirement
OOF shall be declared valid when the Framing Marker is not found during thirteen consecutive frames. OOF shall be declared invalid if the Framing Marker is found twice in two consecutive frames.

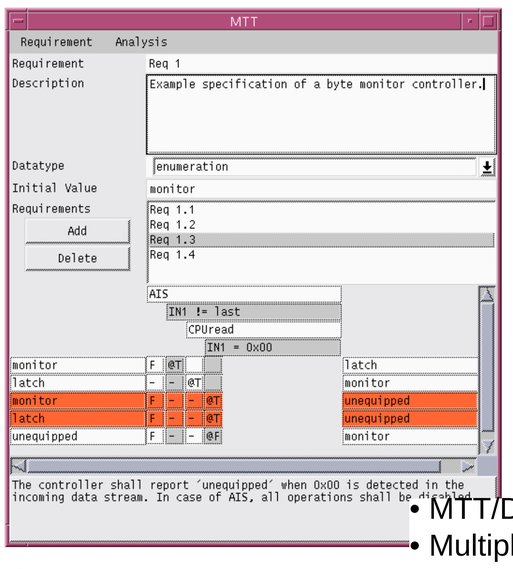
Register Name	Description	Default
OOF	1: FAWfound=0 and frmcnt=13 0: FAWfound=2 and frmcnt=2	0x0
OOFD	1: OOF changed 0: OOFD set to 1	0x0

REQUIREMENT END

ADeVA Language

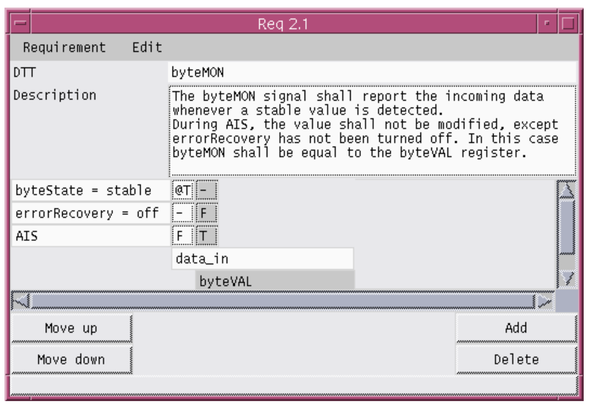
Mode Transition Tables (MTT)

- State machine functionality
- Local view of system behaviour (operation mode)



Data Transformation Tables (DTT)

- New language feature
- Combinational and sequential logic
- Describe manipulation of data signals



- MTT/DTT implicit self assignment if no condition holds
- Multiple events at a time are allowed

Checks

- Syntax checks — wrong cell content
- Integrity checks — all cell objects declared (open ports, signal names, etc.)
- Consistency checks — guarantee of deterministic behaviour (statically reachable, deadlock, cycle detection)

Formal Verification

Model generation

- Implicit priority via IF...ELSIF in VHDL
- Deterministic behaviour of tables requires consis-tency check
  - No endless delta cycles
  - Mapping of table conditions to boolean formulae
  - Conjunction of conditions in a cycle must evaluate to FALSE (SAT problem)

Next steps-creating link to model checker

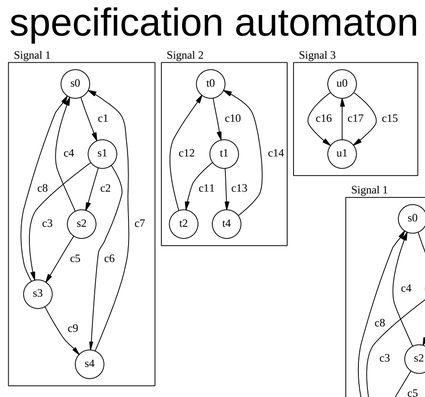
Infineon CVE toolset

- Observation windows
- Property language
  - abstractions
  - coordination
  - safety properties
  - liveness properties
  - counter example generation
- Asynchronous model

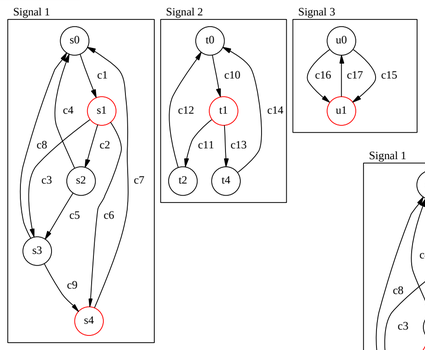
```
ARCHITECTURE behave OF dtt_bytemon I
   -- temp signals
   SIGNAL bytestate_eq_stable: boole
   SIGNAL errorrecovery_eq_off: bool
BEGIN
 bytestate_eq_stable <= true
       WHEN bytestate = e_stable
       ELSE false;
 errorrecovery_eq_off <= true
       WHEN errorrecovery = e_off
       ELSE false;

 PROCESS(bytestate_eq_stable,
         errorrecovery_eq_off, ais,
         data_in, byteval)
 BEGIN
  IF bytestate_eq_stable'EVENT
     AND bytestate_eq_stable = true
     AND ais = false
   THEN bytemon <= data_in;
   ELSIF errorrecovery_eq_off = false
         AND ais = true
   THEN bytemon <= byteVal;
   END IF;
 END PROCESS;
END behave;
```

Automat. Testcase Generation

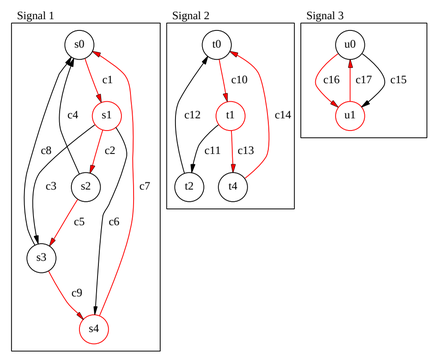
specification automaton



substate selection



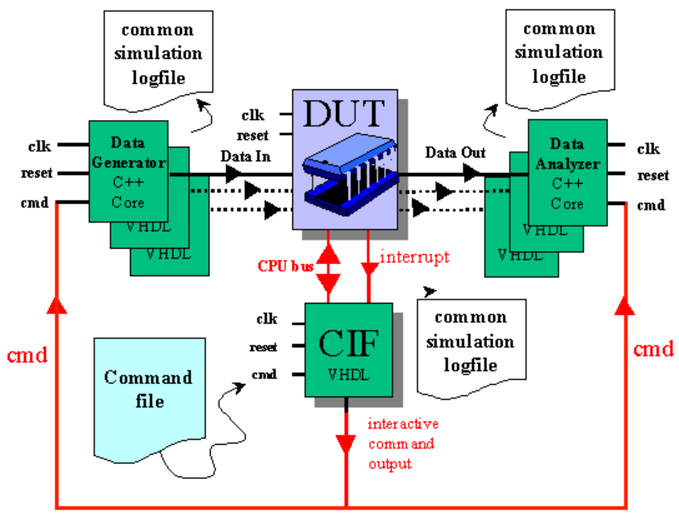
automatic path selection



Procedure:

Generation of an abstract (graph) model of the system
Identification of relevant substates (e.g. system outputs)
Paths in the abstract model correspond to system stimuli
Result
abstract testcases that have to be mapped to the concrete simulation environment

Testbench Concept



- Mixed VHDL/Verilog/C++ Testbench
  - Cadence ncsim
  - Model Technology MTI
  - IKOS hardware accelerator
- Device Under Test (DUT)
  - VHDL RT level, Verilog gate level
- CPU Interface (CIF)
  - C++ core
  - Simulation control
  - Command file interpreter
- Main Data Channel
  - C++ core
  - Sonet/SDH Data Generator & Analyzer
  - Dynamic generation & analysis
  - Nested generators/analyzers
- Secondary Data Channels
  - Overhead access channel, etc.
  - VHDL behavioural models
- Single common logfile
  - time and/or frame based

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