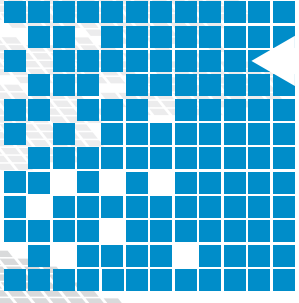
Program

CATRENE / MEDEA+
Design Technology Conference

jointly organized



edaWorkshop **09**

www.edacentrum.de/edaworkshop

Dresden (Germany), May 26 – 28, 2009

About edaWorkshop and CATRENE/MEDEA+ DTC

The edaWorkshop is the premier German EDA event for the publication and discussion of application-oriented EDA research findings. It is also the primary platform for presenting and exchanging solution approaches and results of EDA projects funded by the BMBF (Federal Ministry of Education and Research). The edaWorkshop is organized jointly by the edacentrum and BMBF, DLR and the GI/GMM/ITG RSS Steering Group for "Computer-aided Circuit and System Design".

In 2009, the edaWorkshop will co-locate and share a common day – including keynotes, sessions and the social event – with the annual CATRENE/MEDEA+ Design Technology Conference (DTC), successor of the MEDEA+ Design Automation Conference. The CATRENE/MEDEA+ DTC, is the meeting point of Europe's scientists and experts in application-oriented design. Leading research and development in design automation has been supported by MEDEA+, now by CATRENE, and EUREKA member states during the past ten years.

Both events are attracting European experts in industry and academia and consequently the organizers decided this year to co-locate the workshop and the conference. The mix of representatives from industry and academic research creates ideal opportunities for a professional exchange of ideas on a scientific basis. The dialog can pave the way for industry to benefit from research results. It promotes communication between EDA experts and public authorities, and supports the dissemination of the results of publicly-funded projects.

The three days event is a balanced combination of information and communication. It not only offers a wide range of discussions on specialized subjects and EDA research projects, but also provides several networking opportunities. Furthermore all attendees are invited to contribute to future updates of the multi-annual strategic plan (MASP) of the European research initiative ENIAC. Their input will be collected during the poster exhibition and provided to the funding authorities and ENIAC. This is supported by a comprehensive poster exhibition, where demonstrations and prototypes will also be presented and by the successful cooperation marketplace entitled "Ideas in search of users – market in search of innovations".

Looking forward to seeing you in Dresden!

Prof. Dr. W. Rosenstiel
General Chair

The edaWorkshop and CATRENE/MEDEA+ DTC – Catalyst of EDA Research

The design of integrated circuits and systems places enormous demands on R&D engineers and the design methods and tools that they use. It requires the efficient and manufacturing-aware development of safe, economical, robust and reliable systems of high complexity with very small structures (< 90 nm), and the design of analog and mixed-signal circuits.

In order to stimulate EDA research activities to deal with these challenges, the BMBF (Federal Ministry of Education and Research) has established as part of its research program IKT 2020 an R&D program on design platforms for complex applied systems and circuits. In these IKT 2020 EDA-projects industry and research join forces with the public authorities to support those areas that are vital for the competitiveness of the German industry. There are five application fields with a potentially high added value, and with considerable potential for job creation: automotive/mobility, mechanical engineering/automation, health/medicine, logistics/services and energy/environment.

In many cases the projects on these application fields include European-wide collaboration, they are contributing to the research program of MEDEA+ or CATRENE. The programs of IKT 2020, MEDEA+ and CATRENE complement each other and offer a lot of valuable synergies. This event is a central platform for exchanging information concerning the approaches and results of IKT 2020 projects and of MEDEA+ and CATRENE projects as well. People involved in the projects are invited to present their results by means of talks and posters. At the heart of these presentations will be the relevance of the applications to topics affecting society (as defined in IKT 2020 and CATRENE White Book, part B). As second essential part of the event, the project presentations will be supplemented by a selection of peer-reviewed scientific papers on R&D results.

This year the edaWorkshop is jointly organized with the CATRENE/MEDEA+ Design Technology Conference (CATRENE/MEDEA+ DTC), providing a comprehensive overview of latest algorithms and tools, emerging technologies, key and partially common CATRENE/MEDEA+ and IKT 2020 projects, as well as advanced research in application-oriented SoC design automation in Europe. The joint event consists of a CATRENE/MEDEA+ DTC day (May 26), an edaWorkshop day (May 28), and a joint day common to both (May 27).

Federal Ministry of Education and Research

edacentrum

ITG

GMM

MEDEA+

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- J. **Haase**, edacentrum
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- V. **Schanz**, ITG in VDE
- R. **Schnabel**, VDE/ VDI-GMM

Organization Committee

Giovanni De Micheli: "System-level Design Technologies for Heterogeneous Distributed Systems"

Abstract:
The ongoing scaling and hybridization of manufacturing technologies enables us to attain unprecedented levels of performance as well as to integrate electronic and fluidic circuits with sensors and actuators.

Smart micro/nano systems will be the building blocks of wearable and ambient systems, that gather and integrate heterogeneous data in real time and operate and communicate in a wireless and ultra low power mode.

These systems will foster a revolution in health and environmental management, with the final objective of improving security and quality of life. At the same time, they will create a large market of components and systems, and a renewed perspective for electronic design and manufacturing companies.

To accomplish such an ambitious goal, new technologies and architectures must be matched and tailored to the operational environment by solving novel and challenging design and optimization problems, through the creation of novel design methodologies and tools.

Curriculum Vitae:
Giovanni De Micheli is Professor and Director of the Institute of Electrical Engineering and of the Integrated Systems Centre at EPF Lausanne, Switzerland. He also chairs the Scientific Committee of CSEM, Neuchatel, Switzerland. Previously, he was Professor of Electrical Engineering at Stanford University.

His research interests include several aspects of design technologies for integrated circuits and systems, such as synthesis, hw/sw codesign and low-power design, as well as systems on heterogeneous platforms including electrical, micromechanical and biological components. He is author of: Synthesis and Optimization of Digital Circuits, McGraw-Hill, 1994. Prof. De Micheli is the recipient of the 2003 IEEE Emanuel Piore Award for contributions to computer-aided synthesis of digital systems. He is a Fellow of ACM and IEEE. He is currently Division I Director of IEEE.

Dominique Henoff : „3D Integration for Multimedia Applications“

Abstract:
Multimedia applications are facing new challenges with embedded networking features and 3D needs, graphic and vision. These features are creating challenges in term of systems, architecture split, signal integrity, power dissipation and thermal effects. Interconnect limits, reached with wire bonding, are opening new areas with conceptual changes pushing the 3D integration adoption in a “More Than Moore” way. The 3D integration should be strongly linked with efficient cost analysis and with new EDA solutions.

Interconnect delays with good signal integrity are pushing major design changes: high bandwidth memory interfaces, architectural CPU/bus/caches split and mixed integration with different domains. DDR interfaces in multimedia are sooner breaking the 1Gbps barrier with very low clock jitter. The “More Moore” CMOS scaling copes with larger integration for System on Chip (SoC), nevertheless inter die RC delay cannot follow the move. Beyond flip-chip solder bump, the move to finer pitch bumps is pushing the product integration with the substrate/package/board constraints inside SoC architecture.

A new EDA solution system with higher level language and modelling is required. The bulk of the solution should be an user centric approach taking the benefit of previous experience. The basic approach is to have an early accurate cost evaluation of systems enabling the architecture split, which then gives an accurate schedule on developments made concurrently.

A multimedia product has to cope with very dynamic markets. Multimedia products are taking the benefit of validated HW and SW solutions to address new needs with new concepts. Right cost at the right time is a key for multimedia applications.

Curriculum Vitae:
Dominique Henoff is director of Advanced Technology and Innovation in Home Entertainment Group at STMicroelectronics. His responsibilities include process choice, design solutions, SoC architecture development and associated EDA tools. He started his career in MATRA then BULL on microprocessor systems and VLSI design. In 1994, he joined STMicroelectronics on the 64bit microprocessor development then move in 1999 in US, as program manager, for the SH5 with Hitachi. Back to Europe in 2002, he developed design solutions for nanotechnologies then managed MPEG4 SoC designs.

Klaus Revermann : „Function-oriented Development“

Abstract:
In the automotive market, the demand for electrical and electronic innovations and variations has been growing for some years. Using modular design for components and systems makes it possible to meet this demand for innovations and increased variety.

The number of complex, distributed systems is constantly increasing. A wide variety of factors, such as convenience functions or legal requirements, affect market penetration. Car makers themselves decide how to position themselves on the market by defining the functional scope of their vehicles. The following two variables are important factors in this context: the quantity of functions and the time at which the functional scope is decided.

One key to mastering the current challenges is function-oriented development and the related processes.

Sensibly combining functional orientation and module strategy determines the usability of functions in several models. New processes and modified roles are needed to combine module strategy and functional orientation, which often serve different purposes.

Curriculum Vitae:
Klaus Revermann is Head of Body Electronics and Components at Volkswagen's Technical Development. His area of responsibility encompasses on-board computers, access systems, motorised convenience functions, aerials and component integration. After earning a degree in electrical engineering from Bielefeld University of Applied Sciences in 1994, Revermann worked at Continental ISAD Systems GmbH as a development engineer, focusing on integrated starter/generator systems.

In 1999 he joined Volkswagen AG as a development engineer, working in the area of batteries, generators and integration. Revermann then managed the sub-department Switches and Sensors until he went on to assume leadership of the department Whole Vehicle Electrical System and Infotainment Development at Skoda Auto in the Czech Republic in 2004.

edaWorkshop09 and CATRENE/MEDEA+ DTC Topics

System Level and Hardware/Software Design of Embedded Systems

- Application-oriented EDA
- Specification- and Model-based Design
- ESL Virtual System Design
- Rapid System Prototyping
- Architectural Synthesis and Optmization
- Advanced Architectures (ASIPs, SoCs, MPSoCs, NoC, SiPs and Reconfigurable Architectures)
- IP Reuse
- Development and Optimization of Hardware-dependent Software
- Transaction Level Modeling and Simulation
- Analysis and Optimization of Performance and Power

Analog- and Mixed-Signal Design

- Design Automation for Analog Circuits
- Simulation and Verification
- RF Circuits, Smart Power Circuits
- Model Generation
- Parasitics and Interconnects, Signal Integrity

Test and Reliability

- Innovative Test Methods
- System and Industrial Test
- Design for Reliability, Design for Testability and BIST
- Test Generation, Diagnosis and Fault Modeling
- Statistical, Physical and Defect-oriented Testing
- Test of Regular Structures

Manufacturing-aware Design

- Logic- and Technology-dependent Synthesis for Deep-Submicron Circuits
- Physical Design and Verification
- EMC and Packaging
- Design Centering and Yield Optimization (DfM)
- Statistical Timing Analysis and Variability
- TCAD

Design, Verification and Validation

- Simulation Acceleration
- Formal Verification
- Timing Analysis
- Low Power Design, Analysis and Optimization
- LogicSynthesis and Optimization
- Rapid Prototyping
- Design Productivity

Registration

The participation fee includes 3 days conference, 3x lunch, 2x dinner, conference beverages and conference documents. This is an all-inclusive package. Items are not available separately.

Registration	until May 11, 2009	after May 11, 2009
Participation fee (All prices plus 19 % VAT)	EUR 335,–	EUR 395,–

Payment is possible by bank transfer or credit card: MasterCard, VISA or AMEX.
Registration deadline is on May 18, 2009.

To register choose the registration online (http://www.edacentrum.de/edaworkshop/online-registration) or fax the registration form to +49 511 762-19695.

For questions please contact: Ms. Maren Sperber, fon +49 511 762-19699, sperber@edacentrum.de

Cancellation (only by written request) is possible free of charge until May 11, 2009. Until May 18, 2009, half of the participation fee is retained. After this date the entire participation fee is due.
A replacement for the registered participant with the same affiliation is possible at any time.

Contact

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Tuesday, May 26, 2009

	Welcome and Keynote Moderator: W. Rosenstiel (edacentrum)
10:00	**Welcome** H. Bossy (BMBF)
10:15	**System-level Design Technologies for Heterogeneous Distributed Systems** G. De Micheli (EPFL)
11:00	**Coffee Break**
	Technical Session: System Level Design Moderator: F. Petrot (TIMA)
11:30	**Integrated Analog-Digital HW/SW Co-Design** N. Bannow (Bosch)
12:05	**Industrial Experience with System Level Design** M. Martinez (DS2)
12:30	**TSAR: Virtual Prototyping of a Scalable Multi-core Architecture** A. Greiner (U Pierre et Marie Curie)
12:55	**Q&A**
13:00	**Lunch**
	Technical Session: 3D Integration Design & Technology Moderator: M. Diaz-Nava (STMicroelectronics)
14:00	**Potentials of 3D Integration Technology and Challenges for Design Support** J. Weber (Fraunhofer IZM), P. Schneider (Fraunhofer IIS/EA)
14:35	**3D Technologies and Data Structures – An Overview** R. Fischbach (TU Dresden)
15:00	**CAD Tools and Design Flow for 3D Integration** L. McIlrath (R3Logic)
15:25	**Q&A**
15:30	**Coffee Break**
	Session: LOMOSA/COMCAS Low Power Solutions Moderator: M. Coppola (STMicroelectronics)
16:00	**A Power Aware Transactional Level Multiprocessor Soc Simulation Environment** F. Petrot (TIMA)
16:35	**Novel Method for Power Optimization in Cellular Baseband Circuits** D. Mueller (ST Ericsson)
17:00	**Power-Efficient Routing Implementation in Heterogeneous On-chip Networks** J. Flich (U Politecnica de Valencia)
17:25	**Q&A**

	Panel Moderator: J. Borel (J.B - R&D)
17:30	**TSV (Through Silicon Via) Technology as a Driver for ESL Design Solutions?** The purpose of the panel is to discuss the importance of an ESL concurrent design solution to develop better early optimized products versus present TSV designs using only a bottom up approach. A. Asenov (U Glasgow) M. Coppola (STMicroelectronics) D. Henoff (STMicroelectronics) R. Lauwereins (IMEC) P. Schneider (Fraunhofer IIS/EA)

	Conference Dinner
19:30	Meeting point at hotel reception
19:45	Arrival at „Italien Village“
20:00	**Dinner**
23:00	End of 1st day

Wednesday, May 27, 2009

	Keynote Moderator: J. Haase (edacentrum)
9:00	**3D Integration for Multimedia Applications** D. Henoff (STMicroelectronics)
9:45	**Coffee Break**
	Technical Session: **Design and Verification of Analog/Mixed-Signal Circuits and Systems** Moderator: R. Popp (edacentrum)
10:10	**VeronA Paves the Way for Advanced Verification of Analog Circuits** P. Jores (Bosch)
10:40	**Joint Property Specification for Transient Simulation and Formal Verification of Analog Circuits** S. Steinhorst (U Frankfurt)
11:00	**SystemC-AMS for the Design of Complex Analog Mixed Signal SoC's** K. Einwich (Fraunhofer IIS/EAS)
11:20	**Modeling Heterogeneous Systems with SystemC-AMS: Application to Wireless Sensor Network** F. Pêcheux (U Pierre et Marie Curie)
11:40	**Q&A**

	Poster Session Moderator: C. Hansen (edacentrum)
11:45	**Introduction to the Poster Exhibition** including the project „Synthesis-supported Design of Analog Circuits" (SyEnA)

	Poster Exhibition
12:05	For detailed information see next page.
12:30	**Lunch and Poster Exhibition**
	Technical Session: Design for Yield Moderator: G. Georgakos (Infineon)
14:00	**Yield Optimization and Assessment Methodologies in Physical Design** H. Melzner (Infineon)
14:35	**Challenges in Analog Sizing for Yield and Reliability** H. Gräb (TU München)
15:00	**Waveform-based Timing Analysis for Digital Circuits Using Current Source Models and Model Order Reduction** C. Knoth (TU München)
15:25	**Q&A**
15:30	**Coffee Break**
	Panel Moderator: H. Rödig (Infineon)
16:00	**R&D Ecosystem to Build the European Electrical Car** C. de Vries (NXP) J. Langheim (STMicroelectronics) P. van Staa (Bosch)
17:30	**Break**
	Social Event
18:00	Meeting point at hotel reception for guided tour
18:15	Guided tour at „VW Transparent Factory"
19:00	Meeting point at hotel reception
19:15	Arrival at „Lesage"
19:30	**Award of „EDA-Medaille 2009"**
19:45	**Dinner**
23:00	End of 2nd day

Thursday, May 28, 2009

	Keynote Moderator: N. Wehn (TU Kaiserslautern)
9:00	**Function-oriented Development** K. Revermann (Volkswagen)

	Autonomous Integrated Systems Moderator: V. Schöber (edacentrum)
9:45	**Reliability and Safety-Guarantees in Modern MPSoCs with Real-Time Requirements** M. Sebastian (TU Braunschweig)
10:10	**ESL Power Estimation for Embedded Processors** B. Sander (FZI)
10:35	**A Demonstration Platform for Autonomous Integrated Systems** N. Wehn (TU Kaiserslautern)
11:10	**Coffee Break**
	Poster Exhibition
11:10	For detailed information see end of this page.
13:00	**Lunch**
	Test, Reliability and Validation Moderator: E. Barke (edacentrum)
14:30	**MAYA - A Significant Step for Efficient Production Testing and Faster Yield Learning** F. Pöhl (Infineon)
15:00	**Fault-tolerant Interconnects Using Codes and Self-repair** D. Scheit (BTU Cottbus)
15:30	**A Rapid Prototyping Environment for ASIP Validation in Wireless Systems** M. Alles (TU Kaiserslautern)
15:55	**Closing words** E. Barke (edacentrum)
16:05	End of 3rd day

Poster Exhibition

Poster: **Multi-bit Error Detection for Self-Correcting CPU Pipelines**
A. Bouajila (TU München)

Poster: **A Top-Down formal Verification Approach of LIN Hardware IP based on the GapFreeVerification(TM) Process**
O. Sander (U Karlsruhe)

Demo: **Fast Verification of A/MS-Systems for Automotive Applications**
R. Dölling (Bosch)

Demo: **A Rapid Prototyping Environment for ASIP Validation in Wireless Systems**
M. Alles (TU Kaiserslautern)

Besides these reviewed contributions to edaWorkshop09, the poster exhibition will show posters and demonstrations of all EDA projects funded by BMBF within IKT 2020. Additionally all participants will have the possibility to contribute to the future updates of the multi-annual strategic plan (MASP) of the European research initiative ENIAC.

Program

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Location

Dresden, the capital of Saxony and the former residence of the Wettin dynasty, is a city of art and culture with magnificent buildings, many world-class museums as well as a rich tradition of theatre and music. No book about the history of architecture can forget to mention Dresden's Zwinger Palace. The reconstructed Frauenkirche, the Semper Opera House and the Royal Palace as well as many other historical monuments and collections define the image of the city.

See also: www.dresden.de

The event takes place at the 4-star Dorint Hotel Dresden which is located close to the Old Town. For attendees of the edaWorkshop09 and CATRENE/MEDEA+ DTC edacentrum has arranged special room rates, valid from May 25 – 28, 2009.

Please book your room by April 24, 2009, and mention "edacentrum" as the keyword. After April 24, the fixed quota of rooms for the event will be closed. All participants are kindly asked to make their own hotel reservations directly:

Photo: Mr. Krumnow

Dorint Hotel Dresden
Grunaer Straße 14
01069 Dresden
Germany

Fon +49 351 4915-0
Fax +49 351 4915-100
www.dorint.com/en/hotel-dresden

Special Room Rates at Event Hotel				
Dorint Hotel Dresden	Single room	EUR 110,–	incl. breakfast	Fon +49 351 4915-0
	Double room	EUR 131,–	incl. breakfast	

For alternative hotels see www.edacentrum.de/edaworkshop/location

Directions to the Dorint Hotel Dresden

From the airport

By taxi:
The taxi fare to the hotel is about EUR 16.

By public transportation:
Take S2 local train (direction "Pirna Bahnhof"), get off at "Dresden Mitte". Take tram no. 1 (direction "Dresden Prohlis"), get off at "Deutsches Hygiene-Museum".

See also:
www.dresden-airport.de/en

From the main railway station

Take tram no. 3 (direction "Dresden Wilder Mann"), 7 (direction "Weixdorf") or 10 (direction "Dresden Ludwig-Hartmann-Straße"), get off at "Pirnaischer Platz". Take tram 4 (direction "Dresden Kronstädter Platz") or 12 (direction "Dresden Leutewitz"), get off at "Deutsches Hygiene-Museum".

See also: www.dvb.de

From the west via A4/A14 (Frankfurt/M, München, Leipzig)

Exit no. 77b "Dreieck Dresden West" into motorway A17 (direction Prag/Dresden-Gorbitz), take exit no. 3 into B170 towards "Dresden Zentrum" (approximately 6 km), drive straight ahead up to "Pirnaischer Platz", turn right into "Grunaer Strasse" (direction "Gruna"), after 200 m the Dorint Hotel is on the right side.

From the north/east via A4/A13 (Hamburg, Berlin, Bautzen)

Exit Nr. 81 "Dresden/Hellerau" into B170 towards "Dresden Zentrum" (approximately 7 km), pass the bridge "Carolabrücke", at the 2nd crossroad at "Pirnaischer Platz" turn left into "Grunaer Strasse" (direction "Gruna"), after 200 m the Dorint Hotel is on the right side.

Using a navigation system
Choose "Pirnaische Vorstadt" as district when you enter "Grunaer Strasse".