November, 6-7 2003

edaForum03

edaForum03

Millenium Hotel and Resort
Stuttgart, Germany

edaForum03

Outstanding EDA Experts

Meet outstanding EDA experts and
enjoy discussing your favoured topics!

Keynotes

Listen to keynotes of Giovanni De Micheli,
Andrew B. Kahng, Grant Martin,
Joachim Kunkel and Jacques Benkoski

Key Questions

Find Answers to key questions like
"EDA - Waste of money or key to success?"
"Which system level languages will survive?"
"Design productivity - measure or die?"
"Do we need new design concepts in the
physical hell below 90 nm?"

Company Presentations

See new solutions at various company presentations!

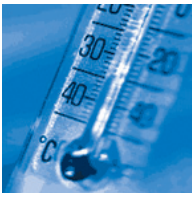
Social Event

Enjoy the exclusive social event
in a typical French styled restaurant.

Trips and Tours

Be guided on different trips and tours, which lead to
beautiful, interesting and exciting places in the region.

Content



Preface

There is no future without microelectronics and there is no microelectronics without EDA. Investment into EDA is not only a cost factor but strategically important for mid and long term ROI. The experts in the field know what Dr. Handel Jones, CEO at IBS, Inc. wrote in his 2002 Study about the IC Industry: „Design Technology Focus Increases IC Vendor Profits." The edacentrum and its annual international edaForum are fully committed to explain and justify the necessity and importance of EDA to decision makers in industry and government.

Again many outstanding speakers from system and microelectronics industry, from EDA vendors, analysts, and academia will share their views with you about technical as well as business related challenges and will give answers to questions like:

How can design productivity really be measured? – Are we trading-off too much cost and flexibility for time-to-market? – What is the ROI of EDA? – Do we need new concepts for the design below 90nm? – What are the implications for technology and tools for more and more heterogeneous designs? – Is ESL design finally ready to join the mainstream? – What system level languages will survive and how can they be used best?

The two parallel tracks of technical and business-related sessions will always be followed by plenary discussion panels.

Before our keynote speaker Prof. Giovanni De Micheli will open the edaForum03 – in this year part of the European EDA Week - we have four interesting parallel vendor presentation sessions. The event will be concluded by the 8th ESCUG meeting as well as by a couple of trips & tours. And last but not least we again will have an exclusive social event with a very special guest.

On behalf of the edacentrum I cordially invite you to attend edaForum03 in Stuttgart. I'm looking forward to interesting talks and discussions and hope to meet you there!

Wolfgang Rosenstiel
Deputy Chairman
edacentrum

Designing Robust Systems with Uncertain Information

Forthcoming technologies for realizing microelectronic systems will be characterized by a large spread of physical parameters. At the same time, systems will experience widely varying environmental conditions according to the time, place and mode of use. The design challenges are direct consequences of the technological progress, and are due to the extremely small nature of electronic devices, the extremely large complexity of systems, and the new unchartered territory set by novel technologies. System robustness and dependability will require the use of new design paradigms to cope with designers' imprecise knowledge of the physical properties of devices and interconnect as well as incomplete knowledge of data traffic.

New, aggressive design methods may address the problem by using self-calibrating circuits and error-resilient computation and communication. Such methods will be based on a design paradigm shift: electrical level information may happen to be corrupted, yet systems will yield reliable services because means are provided to correct for such errors. This keynote will address some of the major challenges of future design technologies and propose new approaches to address them.

Giovanni De Micheli
Professor of Electrical Engineering
and of Computer Science
Stanford University

Giovanni De Micheli is Professor of Electrical Engineering, and by courtesy, of Computer Science at Stanford University. His research interests include several aspects of design technologies for integrated circuits and systems, with particular emphasis on synthesis, system-level design, hardware/software co-design and low-power design. He is author of: Synthesis and Optimization of Digital Circuits, McGraw-Hill, 1994, co-author and/or co-editor of six other books and of over 270 technical articles. He is member of the technical advisory board of several EDA companies, including Magma Design Automation, Coware and Aplus Design Technologies. He was member of the technical advisory board of Ambit Design Systems.

Dr. De Micheli is the recipient of the 2003 IEEE Emanuel Piore Award for contributions to computer-aided synthesis of digital systems. He is a Fellow of ACM and IEEE. He received the Golden Jubilee Medal for outstanding contributions to the IEEE CAS Society in 2000. He received the 1987 IEEE Transactions on CAD/ICAS Best Paper Award and two Best Paper Awards at the Design Automation Conference, in 1983 and in 1993.

He is President of the IEEE CAS Society. He was Editor in Chief of the IEEE Transactions on CAD/ICAS in 1987-2001. Dr. De Micheli was the Program Chair and General Chair of the Design Automation Conference (DAC) in 1996-1997 and 2000 respectively. He was the Program and General Chair of the International Conference on Computer Design (ICCD) in 1988 and 1989 respectively. He was also co-director of the NATO Advanced Study Institutes on Hardware/Software Co-design, held in Tremezzo, Italy, 1995 and on Logic Synthesis and Silicon Compilation, held in L'Aquila, Italy, 1986. He is a founding member of the ALaRI institute at Universita' della Svizzera Italiana (USI), in Lugano, Switzerland, where he is currently scientific counselor.

November, 6th 2003

01.15 pm - 02.15 pm
Room: Berlin 1

DEVIL IN DISGUISE

The Deep Submicron Hell of Physical Design

Keynote

The Design-Manufacturing Roadmap

Designers, EDA vendors, and semiconductor manufacturing equipment vendors have fundamentally conflicting goals, with each community engaged in incremental, linear extrapolation of its current trajectory. To maintain the cost (i.e., value) trajectory of Moore's Law requires the cooperation and co-evolution of these communities. From the EDA perspective, focus areas include
(1) direct, manufacturability-driven optimization of cost and value;
(2) restricted and/or error-tolerant design;
(3) intelligent data preparation;
(4) „analog rules" (as opposed to „digital", 0/1 rules); and
(5) a host of other potential layout and design optimizations.

The basic need is for a „bidirectional design-manufacturing data pipe", driven by cost and value. Design functional intent must be passed to manufacturing, so that incremental manufacturing resources directly improve circuit performance, parametric yield, and/or other measures of product value. Going the other way, models of manufacturing equipment and processes must be passed up to design, so that, e.g., only manufacturable and verifiable layouts will be created. This talk addresses key design challenges for mask, litho and cost-driven product development - as well as a roadmap for design-manufacturing integration.

November, 6th 2003

02.30 pm - 03.15 pm
Room: Bochum/Essen

Is physical design of deep submicron devices designer's hell on earth? What are the devils in disguise there and how can they be scared away?

Andrew B. Kahng is professor in the UC San Diego CSE and ECE departments. He was the founding General Chair of the International Symposium on Physical Design and co-founded the Workshop on System-Level Interconnect Planning. Since 2001, he has chaired the U.S. and international working groups for Design Technology for the International Technology Roadmap for Semiconductors. His research is on physical design and performance analysis of VLSI, as well as the VLSI design-manufacturing interface. In the latter area, results span optimal phase conflict resolution, dummy fill syntheses, min-cost lithographic correction, subfield scheduling for mask write, and generation of compressible layouts.

Andrew B. Kahng
Professor at the Computer Science Department
University of California, San Diego

DEVIL IN DISGUISE

The Deep Submicron Hell of Physical Design

Semi-Hierachical Layout Approaches for ASIC Designs with Multi-Million Instances

During the last years multi-million transistor ASICs with several millions instances have become common. Due to shrinking technology the silicon space on a chip enables more and more System-on-a-chip (SOC) designs. From a physical design point of view these designs often consists of two design levels: First, the „Functional Unit Level", containing either fixed size (custom-) macros or Random Logic Macros (RLMs), which are synthesized independently and therefore are heavily interconnected. Apart from that, these units usually are loosely attached to the remaining logic. Second, the „Chip Top Level" in which the interconnections of Functional Units are done and in which the connection to the outside world is built.
In the past, two major approaches have been established to layout such chips: hierarchical and flat design styles. While the former allows for very quick turn-around-times (TAT) by divide and conquer strategies, the latter minimizes design and manpower overhead and usually results in better overall solutions.
In contrast to most other companies in the industry IBM has favoured the flat approach so far. However, on some of our latest multi-million transistor instances designs IBM has developed methodologies to incorporate hierarchical elements into our flat approach to reduce the increasing TAT while preserving the major advantages of a full flat approach. In this talk these methods and the experiences that have been gained by applying them on some of the largest ASICs in the industry will be presented.

Markus Bühler was born in 1967 at Offenburg/Germany. He studied Electrical Engineering at the University of Karlsruhe from 1987 to 1993. After various industry positions he was research assistant at the University of Stuttgart in the area of Low Power Design. Since 1999 he works in the field of physical design at IBMs ASIC Design Center in Böblingen. Markus Bühler graduated as Dr. rer. nat. from the University of Stuttgart in the year 2000.

Markus Bühler
ASIC Design Center
IBM Microelectronics, Inc.

November, 6th 2003

03.45 pm - 04.15 pm
Room: Bochum/Essen

Design Closure Starts With DESIGN

Design closure is commonly viewed as an activity that happens at the end of the design process. This leads to long, expensive iterations but more importantly results in designs that waste performance, area and power. As was the case with quality, closure cannot be inspected or repaired into a product after the fact. Design closure must start at the beginning of the design process. This talk will focus on the changes in methodology that are needed to enable designers to close their designs at the beginning of the process, thereby producing significantly better designs in much less time and with lower engineering costs.

Jacques Benkoski is the President and CEO of Monterey Design Systems. Under his management, Monterey has grown to over 140 employees, delivered the industry's first complete silicon virtual prototyping product line, expanded to over 30 customers worldwide, and raised over 100 Million US$ in funding.

Prior to Monterey, Dr. Benkoski founded and headed European operations for EPIC Design Technology and then held various senior management positions at Synopsys. He previously held a number of research and management positions at STMicroelectronics in France and Italy, IMEC in Belgium, and IBM in Israel.

Dr. Benkoski also serves as the Vice-Chairman of the EDA Consortium and has been a member of its executive committee for three years, during which he defined and directed the organization's first comprehensive industry outreach campaign. He received a B.Sc. in computer engineering from the Technion, Israel Institute of Technology and M.Sc. and Ph.D. degrees in electrical and computer engineering from Carnegie Mellon University.

Jacques Benkoski,
President and CEO,
Monterey Design Systems, Inc.

November, 6th 2003

04.15 pm - 04.45 pm
Room: Bochum/Essen

INDUSTRIAL DISEASE

Measure or Die - Design Productivity

Keynote

Economics of IP

Ever shrinking silicon geometries and the resulting growing number of transistors that can be implemented on a single die will continue to fuel the trend towards systems on a chip (SoCs). For the same reasons that growing complexity led to the adoption of standards in the world of electronic systems. Standards are also finding their way into SoCs. As a result, an increasing portion of these SoCs can be assembled from pre-designed blocks that implement functionality defined by standards.

This has created a business opportunity for so called IP vendors to develop ‚ready to use' standards-based IP blocks and market them to semiconductor companies who integrate these IP blocks into SoCs. The underlying assumption is that it should be economically more efficient to have a small number of IP vendors develop these IP blocks for the entire industry than each semiconductor company developing them for their own use.

From an IP vendor point of view the fundamental question is how large is the market for a particular new standard. In other words, how many SoCs will need an IP block that implements that standard. This question needs to be answered well before semiconductor companies start sourcing IP blocks for that standard, and many times in light of various new standards competing for the same role. Waiting to see how the market acceptance of these new standards develops is hardly an option. Whoever is first to market with a high quality IP block usually ends up dominating the market.

From the point of view of an IP user, the question is how much of the total cost of developing, verifying, and integrating a particular standards-based function can be saved by procuring it as an IP block, be it from some other department in the same company or from an external IP vendor. Assuming the IP component fits architecturally into the SoC, invariable the all decisive factor is the quality of the IP block. If an externally procured IP component requires, for lack of quality or confidence, to undertake a complete verification effort, much of the expected cost advantage will be lost.

This talk will examine the economics underlying standards-based IP from the perspective of both the IP vendor and that of the user of IP.

November, 6th 2003

02.30 pm - 03.15 pm
Room: Hamburg

„How to measure design productivity?“ - An old question, yet without answer. Do we really know where delays come from, or is this insufficiency in measurement a sign for an industrial disease?

Joachim Kunkel is the Vice President of Engineering and Design Solutions at Synopsys, Inc. Prior to joining Synopsys Joachim was a managing director of CADIS GmbH, a company he had co-founded in 1989 in Aachen, Germany. CADIS GmbH focused on the development of system level design tools for digital signal processing and providing specialized design services for wireless communication systems.

From 1984 to 1989 Joachim was a research assistant at the Aachen University of Technology's "Lehrstuhl für Elektrische Regelungstechnik", where he conducted research in the area of system level simulation techniques for digital signal processing, with special emphasis on parallel computing.
Joachim Kunkel received a "Dipl.-Ing. der Nachrichtentechnik" degree (MSEE equivalent) from the Aachen University of Technology, Aachen, Germany in 1984.

Joachim Kunkel
Vice President of marketing
for IP Design Solutions
Synopsys, Inc.

INDUSTRIAL DISEASE

Measure or Die - Design Productivity

Design Cost Modeling and Data Collection Infrastructure

The 2001 International Technology Roadmap for Semiconductors introduced a new design cost model that highlighted both the cost of design and the benefits of EDA technology. For practical evaluation and optimization of design cost, standard measurement infrastructure is needed. This talk reviews experience with METRICS, an open-source infrastructure developed in the MARCO Gigascale Systems Research Center. METRICS allows instrumentation of design tools and design processes, collection of design artifact and design process data, and prediction of future results and data based on current information. The end goal is a „science, rather than an art" of chip design and implementation - and the key precept is that design processes must be measured before they can be improved. METRICS (1) unobtrusively gathers characteristics of design artifacts, design processes, and communications during the system development effort, and (2) analyzes and compares that data to analogous data from prior efforts. A variety of benefits can result, including resource prediction, go / no-go decision support, project monitoring, design flow debugging and error prevention, benchmarking, and identification of good predictors and new metrics that reflect eventual design success. Example applications in a chip implementation flow will be reviewed.

Andrew B. Kahng is a professor in the UC San Diego CSE and ECE departments. He was the founding General Chair of the International Symposium on Physical Design and will co-chair the Design Automation Conference program committee in 2004. He has also been active in the MARCO Design and Test Focus Center, here his theme has built infrastructures for roadmapping, open-source CAD IP, and metrics collection for design process optimization. His research centers on physical design and performance analysis of VLSI, as well as the VLSI design-manufacturing interface.

Andrew B. Kahng
Professor at the Computer Science Department
University of California, San Diego

November, 6th 2003

03.45 pm - 04.15pm
Room: Hamburg

IBM ASIC Design TAT Reduction

A key factor in the time-to-market for an ASIC design is turnaround time (TAT). Because of the ever-increasing complexity of ASIC designs, a 30% reduction in TAT simply keeps the development time at a constant level in the evolution from one technology node to the next. More time must be shaved from TAT to reduce the overall development time. The base for this improvement was a detailed analysis of the major contributors to design TAT. The improvement presented in this talk, include algorithmic improvements, new sign off criteria, a higher degree of automation and more powerful IT equipment.

Putting all these measures in place, IBM has reduced the time required to process the production netlist by 60% in a two-year window. These TAT reductions and the higher complexity of the 130 nm technologies result in a triple productivity improvement from one technology node to the next.

It will be shown that the main contributors to design TAT changed as a result of this work. The placement and timing closure step with ideal clocks, that dominated the TAT in 2001 is by now no longer the bottleneck and the focus shifted to the percentage of TAT spent on post routing timing and noise closure. The improvements put in place to address this part of the process will be outlined.

Jürgen Koehl studied Mathematics in Bonn and Paris. Prior to joining the IBM development lab in IBM Böblingen in 1989, he was a member of the VLSI research team at the Institute for Discrete Mathematics in Bonn, Germany. Together with IBM's research partners in Bonn he implemented one of the first timing driven design systems which was used for the first IBM CMOS S/390 processors. From 2001 to 2003 Jürgen Koehl was on assignment to Burlington, Vermont to lead the world wide ASIC design turn-around-time reduction for IBM's ASIC Design centers. Currently he is a Senior Technical Staff Member in the IBM ASIC Design Center in Böblingen, Germany.

Jürgen Koehl
Senior Technical StaffMember,
ASIC Design Center Infrastructure
IBM Microelectronics, Inc.

November, 6th 2003

04.15 pm - 04.45 pm
Room: Hamburg

STAIRWAY TO HEAVEN

The 7th Heaven of System Level Design

Keynote

An Overview of System-Level Design: Current Status, Future Possibilities

System-level design has been the once and future hope for electronic design automation for a long time: from ESDA to now ESL, the takeoff is always just about to happen, yet never seems to arrive. However, the design world is changing and the conditions for a wider adoption of system-level design methods and technologies may be far riper now than in the past. We should remember, too, that ‚system' extends far beyond the hardware-centric views of most of EDA, to embrace software, especially in embedded real-time products. System-level design (SLD) has been successfully applied to the design and implementation of dataflow and control algorithms in a number of signal and image processing application domains for many years. Currently, there is a lot of renewed interest in the modeling of System-on-Chip design platforms at higher levels of abs traction. For the future, there are several trends. Effective use of hardware in a software-centric world has re-awoken interest in behavioral synthesis in a new form: co-processor synthesis. New system architectures mean resurgence of interest in the co-design problem, albeit „SW-SW" co-design than „HW-SW". The desirability of bringing the HW and SW worlds together in the new discipline of system design means a closer look at developments in SW modeling and tools, such as the evolution of UML, and its linkage to EDA-based SLD.

Grant Martin is a Fellow in the Labs of Cadence Design Systems. He joined Cadence in late 1994. Before that, Grant worked for Burroughs in Scotland for 6 years and Nortel/BNR in Canada for 10 years. He received his Bachelor's and Master's degrees in Mathematics (Combinatorics and Optimization) from the University of Waterloo, Canada, in 1977 and 1978.
Grant is a co-author of Surviving the SOC Revolution: A Guide to Platform-Based Design, 1999, and System Design with SystemC, 2002, and a co-editor of Winning the SoC Revolution: Experiences in Real Design, and UML for Real: Design of Embedded Real-Time Systems, June 2003. He co-chaired the VSI Alliance Embedded Systems study group in summer 2001. His particular areas of interest include system-level design, System-on-Chip, Platform-Based design, and embedded oftware.

Grant Martin
Cadence Fellow, Chief Technologist for the Sytem Level Design and Verification Group
Cadence Design Systems, Inc.

November, 7th 2003

09.00 am - 09.45 am
Room: Bochum/Essen

Are SoC designers in seventh heaven when using system-level-design? And what about SystemC and SystemVerilog - can they provide a stairway to that heaven?

Virtual Prototyping

Virtual Prototyping of complete Integrated Circuits (ICs) is the key for early HW/SW simulation. Virtual Prototyping means here to run IC software on a model of the IC hardware called Virtual Prototype System before silicon is available.

At Infineon Technologies Secure Mobile Solutions division Virtual Prototype Systems are successfully used for architecture exploration and early software simulation since years. The latest Infineon base-band IC S-GOLD was completely developed by this technology: technology. Thus, architecture exploration & proof was performed on the specification level, while the Software was developed 9 months in advance and runs first time right on silicon.

Our Virtual Prototype Systems are pure C/C++ based models. The systems do not use hardware modeling dialects like SystemC. The main focus is on model reuse within Virtual Prototype Systems and within EDA tools by guaranteed simulation speeds up to several 100 KHz. The backbone of our Virtual Prototype Systems is a C/C++ model API called CommonAPI. This API is common to each Virtual Prototype component/model. It enables smooth integration into third party tools and plug & play construction of Virtual Prototype Systems.

Carsten Mielenz is leading the System Labs Group at Infineon Technologies Secure Mobile Solutions division. He is in charge for HW/SW architecture exploration and definition, system simulation and IP (hardware and software) benchmarking. Prior to these Mr. Mielenz has built up the Virtual Prototype System centre at Secure Mobile Solutions. Before joining Infineon Technologies Mr. Mielenz worked several years for Motorola Semiconductor in the automotive division. There he was focusing on system modeling for car network systems and designed network controller like CAN. Mr. Mielenz received the Dipl. Ing. in Communication Science from the Technical University of Munich, Germany.

Carsten Mielenz
Leader System Labs Group
Secure Mobile Solution Division
Infineon Technologies

November, 7th 2003

09.45 am - 10.15 am
Room: Bochum/Essen

STAIRWAY TO HEAVEN

The 7th Heaven of System Level Design

Transaction Level Modeling in SystemC

This talk will describe the Transaction Levels of modeling within SystemC. The various abstraction levels within Transaction Level Modeling (TLM) are identified, and the overview of the APIs are given. Three main TLM levels will be defined: Programmers View (PV), Programmers View plus Timing (PVT) and Cycle Callable (CC).
Programmers View captures the behavior of the hardware components, as seen by the embedded software developer. The model is bit-true, register accurate, no clock, no timing, enough synchronization to enable correct functionality. Transactions at this level represent information which may be passed over a number of cycles. The interface is blocking and reactive.
Programmers View plus Timing inherits the PV model and includes timing and other benchmarking or debugging information. Additionally, there is synchronization with the system clock. In all other ways, it is identical to the PV. Cycle Callable is clocked, can use abstract data types, and is statically schedulable.
Data is transferred by polling, not by reactive function calls. Transactions at this level represent the information passed in one cycle. Each module is refined to model the cycle behavior of the IP (pipelining, communication protocols and structures, out-of-order computations, split responses, etc.). The talk will give some details of ARM's proposed implementation of these levels and how they fit into a design flow.

Mark Burton gained a BEng in Computer Systems Engineering from Warwick University and his PhD from Leeds University. Since then he has worked at Inmos implementing the ALU for the T9000 Microprocessor. At ACRI he designed and implemented the modeling and validation strategy. While at ARM Mark has been responsible for implementing a number of innovative modeling strategies. He is now the engineering manager responsible for ARM's Models and Modeling Technologies. Mark is also the chair of the OSCI SystemC Transaction Level Modeling Group, which is currently defining how modeling should be done across a number of abstraction levels.

Mark Burton
Engineering Manager
Arm Ltd.

November, 7th 2003

10 .45 am - 11.15 am
Room: Bochum/Essen

System Verilog at the Transaction Level

There is a need to design and verify systems at an abstraction level which reflects some of the architecture and performance of the system under design, without too much detail. The communication between subsystems is usually modeled as transactions.

The traditional hardware description languages, Verilog and VHDL, do not support transaction level models well because they lack all the necessary constructs. Hardware verification languages lack the structural modeling constructs needed to represent the architecture. Programming languages lack the low-level hardware support needed to complete the design flow.

SystemVerilog combines the features of a hardware description language and a hardware verification language, and supports the design and verification of systems at the transaction level. The flexibility of interfacing to C allows the integration of processor models to simulate embedded software. The combination allows a high performance verification of the system architecture.

Peter Flake was a founder and Chief Technical Officer at Co-Design Automation and was the main architect of the SUPERLOG language. His EDA career spans 30 years: he was the language architect and project leader of the HILO development effort while at Brunel University in Uxbridge, U.K., and at GenRad. HILO was the first commercial HDL-based simulation, fault simulation and timing analysis system of the early/mid 1980s. With the acquisition, Peter Flake became a Scientist at Synopsys.
He holds a Master of Arts degree from Cambridge University in the U.K. and has made many conference presentations on the subject of HDLs. He served on the Accellera SystemVerilog committees from their inception.

Peter Flake
Scientist
Synopsys, Inc.

November, 7th 2003

11.15 am - 11.45 am
Room: Bochum/Essen

MONEY

Seed, Care and Harvest - Value Focused EDA

Keynote

The Revenge of Economics over Engineering

Since the inception of Moore's Law in 1965, the pursuit of the latest and greatest semiconductor technology has been synonymous with growth, profitability, and market share. However, recent advances in process technology have dramatically escalated the complexity and cost of engineering, and have cast serious doubts over the wisdom of pursuing technological advance for its own sake. This talk will focus on analyzing the relationship between the cost of engineering vs. the cost of manufacturing, and the increasing importance of design technology to master the complex tradeoffs resulting from the rise in importance of the economical parameters.

Jacques Benkoski serves as the Vice Chairman of the EDA Consortium and has been a member of its executive committee for three years, during which he defined and directed the organization's first comprehensive industry outreach campaign. He received a B.Sc. in Computer Engineering from the Technion, Israel Institute of Technology and M.Sc. and Ph.D. degrees in Electrical and Computer Engineering from Carnegie Mellon University.

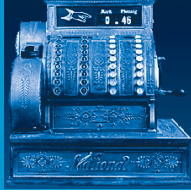
Jacques Benkoski also is the President and CEO of Monterey Design Systems. Under his management, Monterey has grown to over 140 employees, delivered the industry's first complete silicon virtual prototyping product line, expanded to over 30 customers worldwide, and raised over 100 Million US$ in funding.

Prior to Monterey, Dr. Benkoski founded and headed European operations for EPIC Design Technology and then held various senior management positions at Synopsys. He previously held a number of research and management positions at STMicroelectronics in France and Italy, IMEC in Belgium, and IBM in Israel.

Jacques Benkoski
Vice Chairman
EDA Consortium

November, 7th 2003

09.00 am - 09.45 am
Room: Hamburg



It's all about money, isn't it? So what is the right seed and what is the right care for EDA leading to a rich harvest for EDA companies as well as for EDA users?

GLM at Infineon - Effective License Management for Efficient Asset Utilization

In the late 90ies Infineon started to grow faster than the competition and is now on position 6 of all semiconductor companies. Everywhere in the world we founded new Development Centers and hired new designers. These teams at around 35 locations had a strong, never ending "hunger" to a lot and often different EDA design tools. The result was a huge variety of design tools at high costs.

With the general increase of design costs and especially with the downturn of the whole industry cost saving came much more into the focus everywhere. At Infineon Global License Management (GLM) streamlines and optimizes the complete EDA tool usage worldwide. Every demand is gathered centrally and contracts are tailored to meet current usage and future expectation. Different license models (incl. Infineon's favorite one) and their kind of operation will be presented. Conventional models need a lot of administration effort – new ideas are required to reduce this kind of workload.
Cost distribution according to usage guarantees worldwide cost awareness. Flexibility on supplier site is necessary to support a fast changing demand. Following these two principles both parties are the winner: designers with short term technology access AND vendors with easy growing of business.

Klaus Köppel has an over 25 years experience with EDA tools and industry. He started his career as software developer for EDA in-house tools at Siemens (digital simulation, P&R). After 10 years in development and support he moved into the Semiconductor division of Siemens. Responsible for different activities in design and CAD he has gained good insight and a broad overview of the EDA world. With that technical background he started in 2000 to drive the business more from the commercial side: EDA vendor management with contracting and license management offer a lot of possibilities to optimize Return of Investment into EDA technology.

Klaus Köppel
Director
Infineon Technologies AG

November, 7th 2003

09.45 am - 10.15 am
Room: Hamburg

VC Funding for EDA Start-Ups: Pain or Gain? A Founders View

Europe holds a strong position in EDA research, in particular in System-level and mixed signal EDA. National, European and industrially funded research at universities and institutes leads to promising approaches meeting in particular the needs of the European system industry. In many cases the resulting technologies and prototype-tools are the key assets of EDA start-up companies.

We will present an example of such a start-up company founded in 2002 in Oldenburg: ChipVision Design Systems AG. In 2003 the company has successfully closed a venture capital financing round with a syndicate of two renowned venture capital firms. This funding enables to further invest in product development, management and growth.

From the founders' perspective we will briefly summarize the genesis of the company, the stumbling blocks we had to surmount and our perspectives. The presentation will also show the founders' experience and view on this deal.

Wolfgang Nebel holds a degree in EE from Hanover University, Germany, and a Dr.-Ing. degree from the CS department of Kaiserslautern University. From 1987 to 1993 he worked with Philips Semiconductors as a development engineer, project manager and manager of CAD Software Development. Since 1993 he is full professor at Oldenburg University, where he teaches Embedded HW/SW Systems. His research is focused on low power system design methodologies and tools as well as on System-level specification and synthesis. Dr. Nebel is a member of the board of the OFFIS research institute in Oldenburg. He served as Dean of the CS Department and 1st Vice-President of Oldenburg University. Dr. Nebel is Chairman, Chief Technology Advisor and co-founder of ChipVision Design Systems, Oldenburg and San Francisco, CA.

Wolfgang Nebel
CTA
Offis and ChipVision Design Systems AG,
Professor of Electrical Engineering
Oldenburg University

November, 7th 2003

10.45 am - 11.15 am
Room: Hamburg

VC Funding for EDA Start-Ups: Pain or Gain? A VC's perspective?s View

Europe holds a strong position in EDA research, in particular in System-level and mixed signal EDA. National, European and industrially funded research at universities and institutes leads to promising approaches meeting in particular the needs of the European system industry. In many cases the resulting technologies and prototype-tools are the key assets of EDA start-up companies.

We will present an example of such a start-up company founded in 2002 in Oldenburg: ChipVision Design Systems AG. In 2003 the company has successfully closed a venture capital financing round with a syndicate of two renowned venture capital firms. This funding enables to further invest in product development, management and growth.

The presentation will show the VCs' experience and view on this deal. It will explain the concepts of venture capital, decision making processes, and typical general conditions, shed light on the expectations a VC has towards the company's management and founders and add a critical view about the upsides and downsides that accompany a Venture Capital financing.

Andreas Demleitner holds a degree in Industrial Engineering from Karlsruhe University, Germany. Between 1990 and 2001 he worked for Siemens Semiconductors and Infineon Technologies in different functions in Germany, South Africa and California. Positions included responsibility for finance and operations for a business unit in the US and Investment Partner of Infineon Ventures, the Venture Capital arm of Infineon Technologies. In 2001, he joined MergeOptics, a German Fiber Optics startup as co-founder and CFO. Since September 2002, he is responsible for investments in semiconductors and related technologies at BayTech Venture Capital, a renowned Venture Capital Firm based in Munich, Germany. Andreas Demleitner is member of the supervisory board of Xignal Technologies and ChipVision Design Systems.

Andreas Demleitner
Senior Investment Manager
Bay Tech Venture Capital

November, 7th 2003

11.15 am - 11.45 am
Room: Hamburg

Cadence Design Systems, Inc.

Unified Verification Methodology - From System Design to System Design-In

Functionally verifying nanometer-scale ICs requires optimal speed and efficiency. Yet today's fragmented methodologies make it impossible to optimize either. Each verification stage has its own methodology, environment, tools, languages, models, user interface, and APIs. Engineers must re-create almost everything at every stage. The result is a slow, grossly inefficient, expensive process that often allows critical bugs to reach silicon. "Smart" verification techniques that apply to only a single verification stage cannot even begin to address fragmentation. Successful IC design teams need to adopt a unified verification methodology.

Custom IC Platform – From System Specification to Silicon Implementation

Cadence has always viewed Custom IC design as something more than a bunch of point tools. For successful design, there must be a smooth and cohesive flow between the Invention and the Implementation phase of the design. A complete design platform with a high level of automation enabling a seamless top-down design for integrated analog and mixed-signal systems will be presented.

Over the last 6 months, we have taken specific steps to increase the interoperability of the Custom IC tools, both within our own flow and neighboring flows. One of the changes we have made is to identify a method for capturing your design specifications in a central location and be able to always check your design against the specification. Besides this we have also brought in new technology to create a "Silicon Calibrated Library" so that you can start from accurate silicon data and end with first silicon correct. Finally OpenAccess our new common database is designed to allow free IP exchange not only within Cadence but also throughout the industry.

November, 6th 2003

09.00 am - 12.00 am
Room: Bochum, Essen or Hamburg

Doulos Ltd.

Challenges and Solutions for Electronic System Level (ESL) Design

Part 1: The Verification Maze
Current technology allows complex System-on-Chip devices but growth in this area is limited by problems in verifying correct functionality. EDA tools using various languages are emerging to address the verification crisis but the sudden growth of languages has itself caused confusion. We call this The Verification Maze.

This presentation will help navigate The Verification Maze. We present an overview of current tools/methods and explain the jargon. We introduce the languages and present a map of how the EDA tools, methods and languages fit together. Delegates can compare the status and maturity of the tools and languages they may wish to explore further.

Part 2: A SystemC Design Flow for ARM-based Platforms
SystemC allows a complex system to be described at multiple levels of abstraction and systematically refined from abstract algorithm to hardware with embedded software. Debate continues around the intermediate levels of abstraction and refinement methodologies between them.

This presentation will help you understand the SystemC design issues. We describe a methodology and design flow to transform an abstract model into an ARM-based platform. We show how SystemC enables architectural exploration and performance evaluation tasks at an early stage. As the design is refined, delegates will see how the SystemC models and analysis change and at which stages AMBA compliant IP can be used.

The presentation concludes with some comments on the economic impact of SystemC, based on Doulos' experience as training providers to many major electronics businesses across Europe.

November, 6th 2003

09.00 am - 12.00 am
Room: Cardiff

COMPANY PRESENTATIONS

Mentor Graphics Corp.

Verification Languages and where they fit

20 years ago, the EDA industry was dramatically changed by the emergence of new languages that permitted a tenfold increase in design productivity. These were the languages based on RTL principles. While many people described these languages as modeling languages or simulation languages rather than design languages, they were certainly not verification languages and because of this, verification has become a distinct bottleneck in the entire flow. In the last couple of years we have seen the emergence of a new class of languages that are dedicated to verification. This talk will explore some of these trends and how to make sense of the "language wars" that would appear to be erupting.
This technical seminar will review the status quo of system verification in 2003, the languages available today and what engineers can expect in the near future in terms of emerging standards for new verification languages. They definitely make an important part of the foundation for emerging ESL design flows.

Brian Bailey, CTO of the Design, Verification and Test Division at Mentor Graphics Inc. is widely acknowledged as an expert in this field acting as an active member of the Accellera standardization committee.

Verisity Design GmbH

Verification: Can't Live With It, Can't Live Without It

In most companies, "verification" is the dirty little secret of engineering, the poor step-sister of design. Nobody wants to do verification, or if they do, they are put in an isolated cubicle and shunned by the rest of engineering. And managers want to assign the task, then assume it will get done.
The reality is, however, that to be successful with 90nm SoC designs verification must be embraced from the executive level on down. Verification is the Cinderella of the engineering team. Verification should be a core business practice, in the same way that Quality is a core business practice.
There are business implications to this: Verification should be a recognized engineering discipline, with a separate career path in the organization. There should be standard verification engineering practices and methods employed on all projects.

November, 6th 2003

09.00 am - 12.00 am
Room: Bochum, Essen or Hamburg

Verification reuse becomes more important than design reuse. And with verification the key to success at 90nm and below, verification engineers should play a major role in the technical management of projects.
This presentation shows the challenges of verification for 90nm SoCs. A solution to these challenges, System Verification Process Automation (SVPA), is presented. SVPA includes the methodology required to verify from system specification to silicon, and this is discussed. SVPA also includes requirements for managing the verification task, and suggestions for overall business verification practices. Data from several case studies are presented in the areas of developing an organization with verification expertise, implementing verification reuse and managing the verification task.

Synchronicity, Inc.

Building Reuse in an SoC development Envrionment
In the constant reconstruction of today's electronics development environments two main topics have emerged, above the requirement for excellent point tools: the need for the practical Reuse of internal and external Intellectual Property (IP), and its fast, safe and effective use in increasingly complex SoC designs.

Synchronicity has built the mechanisms underlying such environments for most of the top semiconductor fabricators and electronics OEMs. This presentation will illustrate how companies are addressing the control, delivery and (critically) the support of such IP, for internal teams and for their customers' own development groups. It will also describe how these components (hard and soft) can be integrated with work still in progress, across multiple internal and external development teams.

These environments demand the control of the data involved and the best possible communication between all team members on the status/problems/issues/ECOs as they arise, which must be available for management as well as the team members. Examples will be drawn from companies of large and medium size, but all facing the challenges of getting complex designs to silicon as swiftly and safely as possible.

Social Event

Full of Magic: Brasserie Le Jardin

The SI-Entertainment-Center is known for its "Colonnaden": Nineteen themed restaurants and bars which offer exciting wining & dining in different international styles.
We invite you to enjoy the culinary nightlife of the SI-Center and offer you an exclusive evening in the Brasserie Le Jardin – a typical French styled restaurant.

Appropriate to the European EDA-Week a culinary trip through Europe is expecting you with exquisite French cuisine, delights mediterranean and nordish specialities. Beside the excellent dinner buffet, a special guest expects you to take you away to the world of magic and mystery … – Enjoy a delightful and communicative meeting - an exclusive event and great entertainment.

European EDA Week 2003:
MEDEA+ Design Automation Conference 2003
and edaForum03

Investment in EDA will be of crucial importance for the competitive position of the European microelectronics industry. Therefore MEDEA+ and edacentrum jointly organize the European EDA Week 2003 providing comprehensive information on EDA for engineering and management.

The MEDEA+ Design Automation Conference 2003 (Nov 4-6) will present an overview on latest EDA-breakthroughs in different MEDEA+ R&D-projects. In edacentrum's edaForum03 (Nov 6-7) invited speakers will address more business-related topics like return on EDA-investment and will give key messages on system level design and physical design.

MEDEA+

edacentrum

Location

The edaForum03, which is embedded in the European EDA Week, takes place at Stuttgart, Germany, the capital of Baden-Württemberg. The exciting metropolis has the power to charm people with its beautiful squares, palaces and buildings, in all sorts of architectural styles, not to mention its cultural diversity. Top-flight exhibitions, world-famous opera, ballet and drama, variety, musicals and traditional festivals attract millions of visitors every year.

The Stuttgart region is a leading high-tech location in Europe and one of the world's strongest economic centres. It is also home to a large number of international companies such as DaimlerChrysler, Porsche, Bosch, IBM and Hewlett Packard.

Nestling astride the Neckar Valley, the Stuttgart region invites you to experience the exciting and varied range of cultural and leisure activities which take place all year round. Take a boat trip on the Neckar River or in the countryside to the Residential Palace in Ludwigsburg. It is one of the biggest German baroque palaces still around today, is called the "Swabian Versailles" and was the residence of the kings of Württemberg.

More information about Stuttgart
www.stuttgart-tourist.de/english/index.html
www.stuttgart.de

Accommodation

The location of edaForum03 and conference hotel will be the Millennium Hotel and Resort, directly in the SI-Entertainment-Center Stuttgart. The SI-Center is Europe's first urban entertainment centre and a paradise of varieties: the ideal combination of international hospitality, first-class entertainment, exciting restaurants and bars, unique well-being as well as the two world-famous musicals, "Dance of the Vampires" and "The Phantom of the Opera".

www.si-centrum-stuttgart.de/en/

For attendees we have arranged the following special room rates, valid during the edaForum03:

Single room, standard 103 € (+ 15 € Breakfast)
Single room, classic 118 € (+ 15 € Breakfast)

Please book your room until October 3rd, 2003 and mention "edaForum" as keyword. After October 3rd, the fixed quota of rooms for the edaForum is closed. All participants are kindly asked to make their Hotel reservations directly to:

Millennium Hotel and Resort Stuttgart
within the SI-Entertainment Center

Plieninger Straße 100
70567 Stuttgart
Germany
Tel: +49 (0) 711 721 1050;
Fax: +49 (0) 711 721 2931
www.stuttgart.mill-cop.com/

SI-Center Airport Shuttle:
The SI-Center provides a free transport for hotel guests. Please ask the hotel reservation service for details when making your reservation.

Alternative hotels close to the SI-Center
Hotel Körschtal, www.hotel-koerschtal.de
Hotel Gloria, www.hotelgloria.de
Hotel Neotel, www.hotel-neotel.de
Hotel Möhringer Hof, www.hotel-moehringerhof.de

Registration

edacentrum and MEDEA+ jointly organize the European EDA-Week 2003, including the MEDEA+ Conference (Nov 4-6) and the edaForum03 (Nov 6-7). Participants registering for the European EDA-Week are attending MEDEA+ conference plus edaForum03 and are thus enjoying a reduced rate (-20%) for both events.

Participation to:	Until Sept 20	After Sept 20
edaForum03		
edacentrum members	435 €	493 €
Non members,	870 €	928 €
EDA-Week		
edacentrum members	580 €	666 €
Non members	928 €	1014 €

(Prices include 16 % VAT)

The registration form can be found in this booklet.
The edaForum03 participation fee includes forum, Social Event, Trips and Tours, 2x lunch (paid by coupons), conference beverages and conference documents. This is an all-inclusive package. The items are not available separately. edaForum03 participants are invited to participate for free in the edacentrum-Workshop on SystemC embedded in the 8th ESCUG Meeting, November 7, 2003 2 pm - 4.30 pm. For further information check www.edacentrum.de/veranstaltungen

For the edaForum03 the acceptable forms of payment are check, bank transfer, and credit card (Master, VISA or AMEX), while the whole EDA-Week only can be paid by check or bank transfer (compare registration form).

Registration Deadline: October 3, 2003

Please save yourself a place at the edaForum03 and book your room in time because afterwards we could not guarantee vacancy (cf. accommodation). Registrations after the deadline above will be charged with an additional fee of 50 €.

Registrations are processed in the order they are received. Confirmation receipts will be sent via email if an email address is provided. Otherwise, confirmation letters are mailed within 7-10 business days of processing. Please review your registration receipt for accuracy.

Registration

To register, mail or fax the registration form to edacentrum.

edacentrum e.V.
edaForum03 Registration
Schneiderberg 32
30167 Hannover
Germany
fax: +49 511 762 19695

Cancellation
Cancellation (only written request) is possible free of charge until October 17, 2003. Until October 23, 2003 half of the participant fee is raised. There after the entire amount of participation fee becomes due. An agency of the announced participant is possible at any time.

Registration Hours during edaForum03:

November 6, 2003	08:30 am – 04:00 pm
November 7, 2003	08:30 am – 09:30 am
	12:30 am – 02:00 pm

The registration desk will be located in the basement of the building complex "Phantom of the Opera" in front of the meeting room "Berlin".

Information KPN/CVV2/CVC2 of credit cards
The so-called "card-verification value" (CVV2) or "card-verification code" (CVC2) has been added to the rear of the card to help improve security in the remote-transaction sector. We need to have this code for a successful transaction. The value can be found in the signature field, following the printed replica of the credit card number embossed on the front of the plastic. The value is only printed and is not contained in the magnetic-stripe data (in case of American Express cards, the CVV2 is a 4-digit value is to be found half way down the right-hand side of the card).
http://www.edacentrum.de/veranstaltungen/2003/KPN-Info_eng.html

Trips & Tours

Mercedes Benz Sindelfingen – Guided Plant Tour
Württemberg inventors were and still are the driving force behind the successful economic development of the region. The triumphant march of the automobile began here in Stuttgart. Since 1953 the Sindelfingen plant has been offering you the opportunity to collect your new Mercedes-Benz directly from the factory. Experience the highlights of production of a Mercedes-Benz passenger car. The Sindelfingen plant produces vehicles from the C, E, S and CL Class ranges.

A guided tour makes it possible to take a look behind the scenes, which is expected to end at about 4:00 pm.
(Remark: The participation capacity is limited.)
www.mercedes-benz.com/e/about/werke/sifi/werkbesichtigung.htm

TV Tower

The Stuttgart TV Tower is the first TV tower to be built of reinforced concrete. Built in 1954 - 1956 by the architects Leonhardt and prototype for nearly all TV towers throughout the world, Gutbrod and Heinle it stands 217 metres high. With its 4-level "basket" with restaurant and sightseeing platform at 150 metres above the ground and 400 metres above Stuttgart downtown it is a modern landmark. A guided tour through the building gives information about the TV tower, its architecture and its broadcast equipment from the foundation up to its aerials, which is expected to end at about 4:00 pm.
http://www.stuttgart-tourist.de/english/stuttgart/sights/tvtower.html
www.fernsehturm-stuttgart.com

Trips & Tours

State Gallery Stuttgart
The Old State Gallery (1838 - 1843, Architect G.G. Barth) presents art from the Middle Ages up to the 19th century, old German, Italian, Dutch paintings and sculpture from Classic up to Impressionist. The New State Gallery (1979 - 1984 Architect J. Sterling) is recognized today as one of the main works of "Postmodern architecture".

It shows art from the 20th century: main collections Modern Classic: Matisse, Picasso, Beckmann, Schlemmer and art from 1945 onwards: Beuys, Newman, Pollock, Kiefer, Paik and more. Furthermore it has an appealing inner courtyard with sculptures, rooms displaying permanent collections and alternating exhibition rooms. The guided tour through the gallery is expected to end at about 4:00 pm.

www.staatsgalerie.de
www.stuttgart-tourist.de/english/stuttgart/museums/stategallery.html

November 7th, 2003

Additional

8. European SystemC User Group Meeting (ESCUG)
Alternatively to Trips & Tours you can participate the ESCUG-Meeting. The European SystemC Users Group will traditionally provide possibilities for SystemC users to present and discuss their SystemC design experience.
www-ti.informatik.uni-tuebingen.de/systemc/

EDA Achievement Award
The award is confered by the edacentrum to award special research or development efforts in the area of EDA in Germany; especially efforts which have been funded by the German BMBF funding program EkompaSS (design platform for complex applied systems and circuits in microelectronics).

Not a part of the edaforum03 included Trips & Tours but located also in the SI-Entertainment Center and a good opportunity, maybe for a weekend evening:

Phantom of the Opera
Andrew Lloyd Webber's masterpiece at the Palladium Theatre in Stuttgart has fascinated, enchanted and deeply touched over 60 million viewers worldwide. The overwhelming scenery, the splendid décor and costumes and a thrilling story about love and jealousy, glory and honor made "The Phantom of the Opera" one of the most famous musicals of the world.
Information and Tickets: Tel. +49 1805-114 113

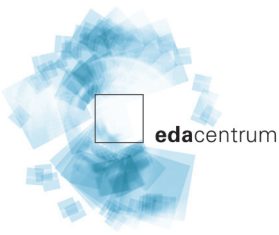
www.stageholding.de or www.phantomderoper.de

About edacentrum

The edacentrum e.V. is an independent association dedicated to the promotion of research and development in the area of electronic design automation (EDA). Its main role is to initiate, evaluate and supervise EDA R&D projects. Further by encouraging basic research projects and EDA networks, it bundles and reinforces the EDA expertise of the German research community. The edacentrum actively engages in public relations in order to sensitize higher management levels, the public and the political arena about the central importance of design automation in microelectronics.

The association helps identify and define research projects on national and international level. In particular, it assists in the preparation and implementation of national and international EDA R&D projects funded by public authorities.

The edacentrum pursues the following strategic goals. It coordinates research and suggests new research topics, channels expertise into effective action and creates new and innovative networks, motivates and consults companies and research institutes in their use of new design methods, secures the processing and steady use of new design tools by assisting in EDA software commercialization, strengthens the market through international cooperation and standardization, supports the BMBF (German Ministry of Education and Research) with its expertise. At present, 29 companies are member of the edacentrum. As an association, the edacentrum e.V. is open to all persons and legal entities.



edacentrum e.V.
Schneiderberg 32
30167 Hannover
Germany

fon: +49 511 762-19699
fax: +49 511 762-19695

Directions

Directions to the Millennium Hotel and Resort located within the SI-Entertainment-Center Stuttgart, Conference location and accommodation.

Arrival by train:
From central station take U5 (to Leinfelden), U6 (to Vaihingen) or U8 (to Möhringen), change at "Möhringen" into U3 (to Plieningen), get off at stop "Salzäcker".
www.bahn.de
www.efa.de

Arrival by plane:
From airport Stuttgart take the SI-Center shuttle:
Please ask hotel reservation service for details,
Tel: +49 (0) 711 721 1050.
Alternatives:
Subway/Train: S2 (to Schorndorf) or S3 (to Backnang), change at "Vaihingen" into U3 (to Plieningen), get off at stop "Salzäcker".
Car: From the airport via B27 direction Stuttgart-Zentrum (city center), exit: "Stuttgart-Möhringen, SI-Center".

Arrival by car
From the A81 motorway, leave at inter-change "Leonberg", to A8 direction Munich, take the motorway exit: "Stuttgart-Degerloch", to B27 direction Stuttgart-Zentrum (city center), exit: "Stuttgart-Möhringen, SI-Center".
From the A8 direction westbound and eastbound respectively, take motorway exit: "Stuttgart-Degerloch", and continue as written above.

www.map24.de
www.hot-maps.de/europe/germany/baden_wuerttemberg/stuttgart/homeen.html
www.stadtplandienst.de

PROGRAM

November, 6th 2003

Registration Opening Time 08:30 am - 04:00 pm

09:00 am — Company Presentations

Mentor Graphics Corp.
"Verification Languages and where they fit"
Room **Bochum/Essen/Hamburg**

Cadence Design Systems, Inc.
"Unified Verification Methodology" and
"Custom IC Platform"
Room **Bochum/Essen/Hamburg**

Doulos Ltd.
"Challenges and Solutions for ESL Design and Verification"
Room **Cardiff**

Verisity Design Inc
"Verification: Can't Live With It, Can't Live Without It"
Room **Bochum/Essen/Hamburg**

Synchronicity, Inc.
"Building Reuse in an SoC Development Environment"

Coffeebreak 10:30 - 10:50

12:00 am — Lunch

01:00 pm — Welcome Address
Erich Barke, Chairman edacentrum

November, 7th 2003

Registration Opening Time 08:30 am - 09:30 am, 12:30 am - 02:00 pm

09:00 am

Technical Session II

Stairway to Heaven
The 7th Heaven of System Level Design
Chairman: Wolfgang Rosenstiel
Room **Bochum/Essen**

Keynote:

"An Overview of System-Level Design: Current Status, Future Possibilities"
Grant Martin
Cadence Fellow, Chief Technologist for the System Level Design and Verification Group
Cadence Design Systems, Inc.

Business Session II

Money
Seed, Care and Harvest - Value Focused EDA
Chairman: Jürgen Haase
Room **Hamburg**

Keynote:

"The Revenge of Economics over Engineering"
Jacques Benkoski
Vice Chairman
EDA Consortium

01:15 pm

Keynote

Room **Berlin I**

"Design Robust Systems with Uncertain Information"

Giovanni De Micheli

Professor of Electrical Engineering and of Computer Science Stanford University

02:15 pm

02:30 pm

Technical Session I

Devil in Diguise

The Deep Submicron Hell of Physical Design

Chairman: Erich Barke

Room **Bochum/Essen**

Keynote:

"The Design-Manufacturing Roadmap"

Andrew B. Kahng

Professor at the Computer Science Department

University of California, San Diego

Business Session I

Industrial Disease

Measure or Die - Design Productivity

Chairman: Peter van Staa

Room **Hamburg**

Keynote:

"Economics of IP"

Joachim Kunkel

Vice president of marketing for IP and Design Services

Synopsys, Inc.

03:15 pm

Coffee Break

Coffee Break

03:45 pm

"Semi-Hierachical Layout Approaches for ASIC Designs with Multi-Million Instances"

Markus Bühler

ASIC Design Center

IBM Microelectronics, Inc.

"Design Cost Modeling and Data Collection Infrastructure"

Andrew B. Kahng

Professor at the Computer Science Department

University of California, San Diego

04:15 pm

"Design Closure Starts With DESIGN"

Jacques Benkoski

President and CEO

Monterey Design Systems, Inc.

"IBM ASIC Design TAT Reduction"

Jürgen Koehl

Senior Technical Staff Member, ASIC Design Center

IBM Microelectronics, Inc.

04:45 pm

Break

05:15 pm

Panel Discussion

Room **Berlin I**

06:00 pm

Break

07:30 pm
11:30 pm

Social Event

European Expeditions full of Magic

Appropriate to the European EDA-Week a culinary trip through Europe is expecting you with exquisite French cuisine, delights mediterrran and nordish specialities. Enjoy a delightful and communicative meeting - an exclusive event and great entertainment.

Restaurant **Brasserie Le Jardin**

09:45 am

"Virtual Prototyping"

Carsten Mielenz

Leader System Labs Group

Infineon Technologies AG

"GLM at Infineon - Effective License Management for Efficient Asset Utilization"

Klaus Köppel

Director

Infineon Technologies AG

Coffee Break

10:15 am

Coffee Break

10:45 am

"Transaction Level Modelling in SystemC"

Mark Burton

Engineering Manager

Arm Ltd.

"VC Funding for EDA Start-Ups: Pain or Gain? A Founder's View"

Wolfgang Nebel

CTO, OFFIS and ChipVision Design Systems AG

Professor of Electrical Engineering

Oldenburg University

11:15 am

"SystemVerilog at the Transaction Level"

Peter Flake

Scientist

Synopsys, Inc.

"VC Funding for EDA Start-Ups: Pain or Gain? A VC's perspective"

Andreas Demleitner

Senior Investment Manager

Bay Tech Venture Capital

11:45 am

Break

12:00 am

Panel Discussion

Room **Berlin I**

Conferment of edacentrum's EDA Achievement Award

01:00 pm

Lunch

02:00 pm

Trips & Tours

Mercedes Benz Sindelfingen – Guided Plant Tour

Experience the highlights of production of a Mercedes-Benz passenger car.

TV Tower

Take a look over Stuttgart from 400 metres above the ground.

State Gallery Stuttgart

See paintings and sculptures from the Middle Ages up to today's postmodern architecture.

8. European SystemC User Group Meeting (ESCUG)

Discuss with SystemC users at the 8. ESCUG-Meeting.

end depending on tour