Challenges and Solutions for Electronic System Level (ESL) Design

by Doulos

Part I: Navigating The Verification Maze

Current levels of silicon integration permit the functionality of an entire electronic system to be integrated onto a single silicon die. However, the growth of the so-called System-on-Chip has been threatened from the outset by the difficulty of verifying functional correctness before committing to manufacture. A range of new EDA tools based around a growing number of proprietary and standard languages is emerging to address the verification crisis, but this sudden growth of new languages has itself caused confusion in the marketplace. We call this The Verification Maze.

This presentation will help you find your way through The Verification Maze. We present a brief overview of current functional verification tools and methods and explain the jargon. We then introduce the current candidate languages in that space, and present a map of how the EDA tools, methods and languages fit together, with the aim of building an understanding of the role and scope of the languages in the verification space. We help delegates to assess the status and maturity of the tools and languages and to reach a view as to which they should explore further.

Part II: Implementing A SystemC Design Flow for ARM-based Platforms

SystemC is an open-source modelling language that is supported by design and verification tools from the leading EDA vendors. It allows the design of a complex system to be described at multiple levels of abstraction and systematically refined from an abstract algorithm to a description of synthesisable hardware with embedded software. However, there is still considerable debate regarding the defining characteristics of intermediate levels of abstraction and how a design should progress through them.

This presentation is based around a case study that will help managers, evaluators and engineers to understand the issues around implementing a design in SystemC. We describe the methodology and design flow followed to transform a generic signal processing system into an ARM-based platform with embedded software. We show how SystemC allows you to perform critical system design tasks such as architectural exploration and performance evaluation at an early stage in the design process. As the design is refined through several levels of abstraction, delegates will see how the nature of the required SystemC models changes, the analysis that can be applied and where standard IP models adhering to the ARM AMBA 2 Transfer Layer SystemC Interface Specification can be used.

The presentation concludes with some comments on the economic impact of SystemC, based on Doulos' experience as training providers to many major electronics businesses across Europe.