

# PROGRAM



## December, 5th 2002

Registration Opening Time 08:30 am - 06:00 pm

|                      |   |  |  |
|----------------------|---|--|--|
| 09:30 am             | <b>Company Presentations</b>  |  |  |
| Coffeebreak          | <b>Mentor Graphics Corp.</b><br>Synthesis and Analysis of Complete Systems  | <b>Cadence Design Systems, Inc.</b><br>System Modelling and Physical Prototyping   | <b>Verisity Design, Inc.</b><br>Functional Verification - One of the Main Challenges in Today's System Designs |
|                      | Room 1  | Room 2   | Room 3   |
| 12:30 am             | <b>Lunch</b>  |  |  |
| 01:30 pm             | <b>Welcome Address</b><br>Erich Barke, Chairman edacentrum  |  |  |
| 01:45 pm             | <b>Keynote</b><br>"The Next Big Advance in Chip-Level Design Productivity"<br>A. Richard Newton<br>Dean of the College of Engineering University of California, Berkeley  |  |  |
| 03:00 pm             | <b>Technical Session I</b><br><b>Titanic Verification of Systems on Chip</b><br>Chairman: Wolfgang Rosenstiel   | <b>Economical Session I</b><br><b>River of no Return EDA and Return on Investment</b><br>Chairman: Andreas Scheffer  |  |
|                      | Room A  | Room B   |  |
| 03:45 pm             | <b>Keynote:</b><br>"The Impending Verification Revolution"<br>Raul Composano<br>Chief Technology Officer, Senior Vice President<br>Synopsis, Inc.   | <b>Keynote:</b><br>"The Strategic Impact of the EDA Industry in the Electronics Design Chain"<br>Guillaume d'Eyssautier<br>Vice President & General Manager Europe<br>Cadence Design Systems, Inc.     |  |
|                      | <b>Coffee Break</b>   |  |  |
| 04:15 pm             | <b>"Tool-Supported Validation of Embedded Systems in Automotive Applications"</b><br>Thomas Kropf<br>Driver Assistance-Function and Software Development<br>Robert Bosch GmbH   | <b>"Bright Longterm Prospects for EDA"</b><br>Peter L. Levin<br>General Partner Techno Venture Management  |  |
| 04:45 pm             | <b>"ROI from Nanometer IC Circuit Verification"</b><br>Sang Wang<br>Chief Executive Officer & Chairman<br>Nassda Corporation  | <b>"An Analysis of the Relationship between EDA Expenditures and Competitive Positioning of IC Vendors"</b><br>Jordan Brysk<br>President & Chief Executive Officer<br>Ascendant Strategies Group, Inc. |  |
| 05:15 pm             | <b>Break</b>  |  |  |
| 05:45 pm             | <b>Panel Discussion</b>   |  |  |
| 06:30 pm             | <b>Break</b>  |  |  |
| 07:30 pm<br>open end | <b>Social Event</b><br>[FJINBOX]<br>The former Finnish Pavilion on the Expo 2000 was coined an "exciting and mystical building". Here you will enjoy dinner with a view over a birch-forest. A musical entertainment will top this exclusive meeting off. |  |  |
|                      | [FJINBOX Expo2000 Plaza]  |  |  |

## December, 6th 2002

Registration Opening Time 08:30 am - 11:00 am

|   |  |  |
|---|--|--|
| <b>Technical Session II</b>   | <b>Economical Session II</b>   | 09:00 am   |
| <b>Gandhi The Dream of Analog Design Automation</b><br>Chairman: Erich Barke  | <b>Modern Times Benchmarking and Productivity</b><br>Chairman: Aidan Kelly   |  |
| Room A  | Room B   |  |
| <b>Keynote:</b><br>"Analog EDA and the Path to Practical Analog IP"<br>Rob Rotenbar<br>Stephen Jatra Professor of Electrical and Computer Engineering Carnegie Mellon University        | <b>Keynote:</b><br>"Methodology and Software for Maximizing Semiconductor R&D Return on Investment"<br>Alexander A. Silbey<br>Director of Professional Services<br>Numeric Management System, Inc. |  |
| <b>"Analog EDA: Is there Light at the End of the Tunnel ?"</b><br>Rudolf Koch<br>Innovations Manager Wireless Solutions<br>Infineon Technologies AG                                     | <b>"The Evolution of Development Processes in the Semiconductor Industry"</b><br>Fritz Kirsch<br>Manager of Design Methodology Group<br>Infineon Technologies AG                                   | 09:45 am   |
| <b>Coffee Break</b>   |  |  |
| <b>"Modeling and the Road towards True Synthesis of Analog Integrated Circuits"</b><br>Georges G.E. Gielen<br>Professor of Electrical and Engineering<br>Katholieke Universiteit Leuven | <b>"Investment into EDA, Its Measurable Success and its Return: The IBM Way"</b><br>Bernd-Josef M. Huettl<br>Marketing Manager<br>IBM Microelectronics   | 10:15 am   |
| <b>"The Return of the Transistor"</b><br>Thomas Heydler<br>Chief Executive Officer<br>Barcelona Design, Inc.  | <b>"Full Custom Mixed-Signal-ASICs-Development: A Determinism of Art"</b><br>Peter van Staa<br>Director<br>Design of Integrated Circuits<br>Robert Bosch GmbH                                      | 10:45 am   |
| <b>Break</b>  |  |  |
| <b>Panel Discussion</b>   |  |  |
| Room Atelier  |  |  |
| <b>Lunch</b>  |  |  |
| 01:00 am  |  |  |
| <b>Trips &amp; Tours</b>  |  |  |
| <b>Rain Forest House</b><br>In the Hannover Rain Forest House you can see, hear, smell, taste and feel the diversity of the tropical highland rain forest.                              | <b>Sprengel-Museum</b><br>See a comprehensive Collection and diverse programme of temporary exhibitions, ranking among the major art museums of the 20th century.                                  | <b>Learning Lab Lower Saxony</b><br>L3S is a center of competence where co-operative research projects, which focus on "collaborative learning technologies for lifelong learning", are carried out. |
| 02:30 pm  |  |  |
| 05:00 pm  |  |  |