System Level Design in the MEDEA+/Ekompass Project SpeAC

Programme

Friday, February 20, 2004

8:30 - 8:45	Registration, Welcome
8:45 - 9:15	New System Level Design Methodologies in the SpeAC Project *W. Rosenstiel*, FZI Karlsruhe, Germany
9:15 - 9:45	Highlights from the MEDEA+ Project A502 MESA *P. Garcin*, ST Microelectronics, France
9:45 - 10:05	Specification and Architecture Exploration of DSP Platforms *B. Candaele*, Thales Communications, France
10:05 - 10:25	Transformation of Simulink Models into Synthesizable HDL Descriptions *M. Stark*, Robert Bosch, Germany
10:25 - 10:40	**Coffee break**
10:40 - 11:00	Bridiging the Gap from System Design to Mixed-Signal IC Implementation with SystemC *W. Hartong*, Cadence, Germany
11:00 - 11:20	System Simulation Speedup Combining SystemC-Models and Reconfigurable Hardware *U. Nageldinger*, Infineon Technologies, Germany
11:20 - 11:40	C++-Based Verification Environment: sciPROVE *R. Hoffer*, sci-worx, Germany
11:40 - 12:00	Design Space Exploration for Network Processor Architectures *S. Künzli*, ETH Zürich, Switzerland
12:00 - 13:00	**Lunch**
13:00 - 13:20	The Tension Between Resource Sharing and Predictable Performance in Real-Time SoCs *K. Goossens*, Philips Research, Netherlands
13:20 - 13:40	Component-Based Design Environment for Multiprocessor SoC Platforms *W. Cesario*, TIMA, France
13:40 - 14:00	Systems Engineering and Distributed Design for Space Application *R. Müller*, EADS Astrium, Germany
14:00 - 14:20	Complex SoC Designs: Change or Challenge for SME Service Providers? *P. Ganal*, Tecnotron, Germany
14:20 - 14:40	Concept of an Integration Platform for the Support of Distributed Engineering Methodologies *G. Lutz*, EuroTelematik, Germany
14:40 - 15:00	The Role of Estimations in Inter-Company Refinement Cycles *J. Kruse*, University of Braunschweig, Germany