Preview on the 43rd Design Automation Conference (DAC)

The world's premier event in electronic system design, July 24-28, 2006, at the Moscone Center in San Francisco /USA

The full program schedule will be available on the DAC Web site at http://www.dac.com.

Registration:
Advance conference registration is open since May 8. The advance conference registration discount deadline is June 26.

Cont@ct:
To register for DAC visit http://www.dac.com or call 1-800-321-4573 in the U.S. to request registration materials.

This year's technical program was selected from the record number of 865 regular paper submissions, 78 panel submissions and 18 tutorial proposals DAC received. The result will be a full and varied program of timely technical and business-related sessions that will appeal to the interests of about 10,000 attendees of this annual event.

Special Theme

This year's DAC has adopted a special theme focusing on multimedia, games and entertainment, which will offer attendees and exhibitors an opportunity to participate in a series of technical sessions, DAC pavilion events and special activities on the exhibit floor. These sessions will highlight the design of the latest generation of multimedia, gaming and entertainment systems. Throughout the week, with a concentration on Wednesday, leading technology providers and consumer electronics manufacturers will be represented in the panel discussions and technical sessions. Highlights will include discussions of the issues faced by iPod and the Cell processor, and the technology requirements for 3-D graphics in feature films.

Keynotes

Dr. Hans Stork, Senior Vice President, Chief Technology Officer and Director of Silicon Technology Development for Texas Instruments, will deliver the keynote address on Tuesday, July 25. It is titled, "Structuring Process and Design for Future Mobile Communication Devices." Dr. Stork will demonstrate how such devices are a driving force for continued economies of scaling in design automation. He will discuss the density and speed of sub-50 nm CMOS technology that is enabling mobile communication device design, as well as the process variations, power issues and complexity that require improved modeling of systematic manufacturing variations and design sensitivities.

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