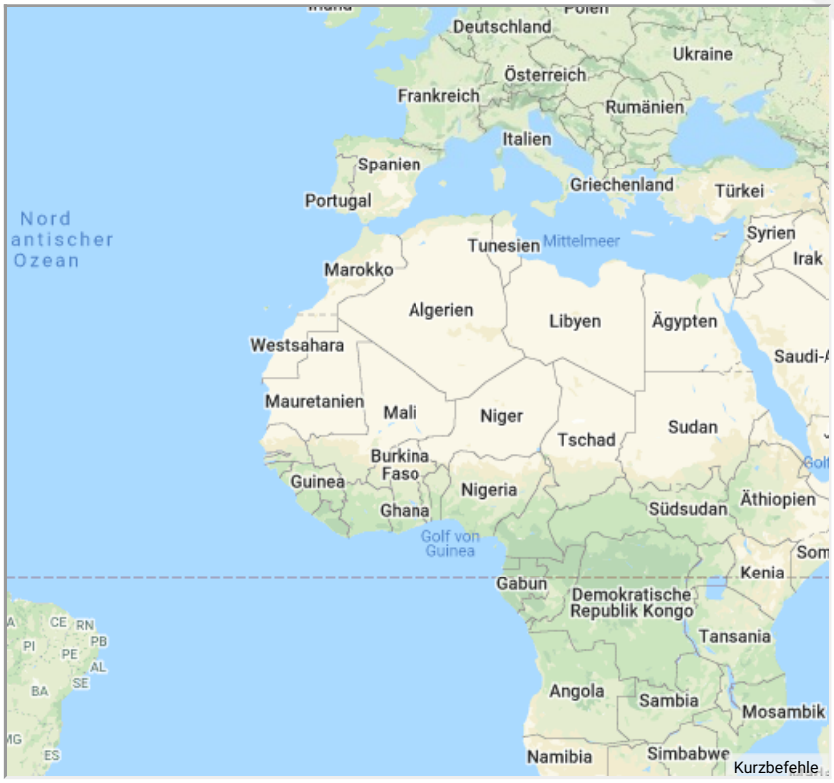
Publications

2020/05/29



1. HNI Newsletter Ausgabe 01 2020 der Universität Paderborn „Neues Verbundprojekt Scale4Edge“. S.8: https://www.hni.uni-paderborn.de/fileadmin/Publikationen/hni_aktuell/hni_aktuell_1_2020.pdf [1]
2. Ecker: Pressekonferenz „Vertrauenswürdige Elektronik“ am 9.6.2020
3. Pressemeldung der TU Kaiserslautern am 6.7.2020
4. Ecker: Silicon Saxony: Vortrag am 11.9.2020
5. Best Paper Award: "Efficient Cross-Level Testing for Processor Verification: A RISC-V Case-Study", Vladimir Herdt, Daniel Große, Universität Bremen, DE, Eyck Jentzsch, MINRES Technologies GmbH, DE, Rolf Drechsler, Universität Bremen, DE, FDL 2020, September 2020
6. Ecker: ZuSE Workshop am 22.9.2020
7. Pressemitteilung IFX, am 24. September 2020 „Projekt Scale4Edge startet im Rahmen der Leitinitiative „Vertrauenswürdige Elektronik“ des Bundesforschungsministeriums - Skalierbares Ökosystem für Spezialprozessoren für das Internet der Dinge wird angestrebt“ (https://www.infineon.com/cms/de/about-infineon/press/press-releases/2020/INFXX202009-090.html [2])
8. Pressemitteilung OSS mit TUK, RB und MNRS, im September 2020
9. Von TUK wurden vier Vortragsbeiträge zum Intel internen SCAP Workshop 2020 (virtuell) eingeladen und geleistet, 28.9.-1.10.2020.
10. Organisation RISC-V Workshop am 8.10.2020
11. Keynote: Invited Talk: RISC-V Scale4Edge Ecosystem - Motivation and Objectives, Wolfgang Ecker (Infineon, D), Workshop on RISC-V Activities 2020, 8.10.2020, Virtuell
12. A RISC-V based Edge Computing Platform with Interchangeable Cores Using 22FDX, Paul Palomero Bernardo, Adrian Frischknecht, Dustin Peterson, University of Tuebingen, D, Workshop on RISC-V Activities 2020, 8.10.2020, Virtuell
13. Energy Efficient RISC-V Implementations in 22 nm, Heiner Bauer (Technical University of Dresden, D), Workshop on RISC-V Activities 2020, 8.10.2020, Virtuell
14. A Compiler Comparison in the RISC-V Ecosystem, Mehrdad Poorhosseini, Kim Grüttner, Wolfgang Nebel (OFFIS, D), Workshop on RISC-V Activities 2020, 8.10.2020, Virtuell

15. Efficient RISC-V Processor Verification via Cross-Level Testing, Vladimir Herdt (University of Bremen / DFKI, D), Eyck Jentzsch (MINRES Technologies, D), Daniel Große (Johannes Kepler University Linz, AT), Rolf Drechsler (University of Bremen / DFKI, D), Workshop on RISC-V Activities 2020, 8.10.2020, Virtuell
16. A Configurable Virtual Prototyping Environment for Different RISC-V ISA Subsets, Peer Adelt (University of Paderborn, D), Workshop on RISC-V Activities 2020, 8.10.2020, Virtuell
17. Security Issues in Hardware/Firmware interaction – Can a formal analysis of (just) the hardware help?, Johannes Müller (Technical University of Kaiserslautern, D), Workshop on RISC-V Activities 2020, 8.10.2020, Virtuell
18. Ecker: Vorstellung von Scale4Edge von auf der EFECS 2020, 25.-26.11.2020
19. UltraTrail: A Configurable Ultralow-Power TC-ResNet AI Accelerator for Efficient Keyword Spotting by Paul Palomero Bernardo, Christoph Gerum, Adrian Frischknecht, Konstantin Lübeck, and Oliver Bringmann, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 39, Issue: 11, Nov. 2020, http://dx.doi.org/10.1109/TCAD.2020.3012320 [3].
20. RISC-V Summit 2020 with "Scale4Edge project introduction" by Wolfgang Ecker, Lead Principle Engineer, Infineon Technologies, Virtual Event, Tuesday, 8 December 2020 12:00pm - 12:20pm - PST (Pacific Standard Time, GMT-8); https://tmt.knect365.com/risc-v-summit/ [4]
21. Kunz, M. Fadiheh: “A Formal RTL Verification Approach for Detecting Transient Execution Side Channels in Processors”, Intel – **IPAS Tech Sharing Forum**, Dezember, 2020
22. Vortrag auf der **Onespin User-Konferenz** OSMOSIS 2020: W. Kunz: “Hardware Security Verification using Unique Program Execution Checking”, 1.-2.12.2020, (virtuell).
23. UltraTrail: A Configurable Ultra-Low Power TC-ResNet AI Accelerator for Efficient Keyword Spotting by Paul Palomero Bernardo, Christoph Gerum, Adrian Frischknecht, Konstantin Lübeck, and Oliver Bringmann, IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, http://dx.doi.org/10.1109/TCAD.2020.3012320 [3].
24. GLSVLSI 2020: "**Verification of Embedded Binaries using Coverage-guided Fuzzing with SystemC-based Virtual Prototypes** ", UB
25. ATVA 2020: "**RVX - A Tool for Concolic Testing of Embedded Binaries Targeting RISC-V Platforms** ", UB
26. ICCD 2020: "**Adaptive Simulation with Virtual Prototypes for RISC-V: Switching Between Fast and Accurate at Runtime** ", UB
27. Vladimir Herdt, Sören Tempel, Daniel Große, and Rolf Drechsler. 2021. **Mutation-based Compliance Testing for RISC-V**. In 26th Asia and South Pacific Design Automation Conference (ASPDAC ’21), January 18–21, 2021, Tokyo, Japan. ACM, New York, NY, USA, 6 pages. https://doi.org/10.1145/3394885.3431584 [5]
28. Vortrag und Panel Diskussion: Wolfgang Ecker “European collaboration: Scale4Edge project introduction”, SOC HUB LAUNCH – BOOST COMPETITIVENESS THROUGH SYSTEM-ON-CHIP at Tampere. Smart City Week, Online, 27.01.2021, https://smarttampere.fi/en/home/ [6]
29. **An Effective Methodology for Integrating Concolic Testing with SystemC-based Virtual Prototypes** , Sören Tempel1 Vladimir Herdt1;2 Rolf Drechsler1;2, 1Institute of Computer Science, University of Bremen, Bremen, Germany, 2Cyber-Physical Systems, DFKI GmbH, Bremen, Germany, DATE 2021
30. **Extending Verilator to enable Fault simulation** , Endri Kaja[1,2], Nicolas Ojeda Leon [1,4], Michael Werner [1,3], Bogdan Andrei-Tabacaru [1], Keerthikumara Devarajegowda[1], Wolfgang Ecker[1,3], [1]Infineon Technologies AG, Germany, [2]Technische Universität Kaiserslautern, Germany, [3]Technische Universität München, Germany, [4]Darmstadt University of Applied Sciences, Germany, MBMV, Virtuell, 18.-19.3.2021.
31. **On Self-Verifying DSL Generation for Embedded Systems Automation** , Zhao Han1,2, Shahzaib Qazi2, Michael Werner1,2, Keerthikumara Devarajegowda1,3, Wolfgang Ecker1,2, Infineon Technologies AG1 - Technical University Munich2 - Technical University Kaiserslautern3, MBMV, Virtuell, 18.-19.3.2021.
32. **Register and Instruction Coverage Analysis for Different RISC-V ISA Modules** , Peer Adelt, Bastian Koppelmann, Wolfgang Mueller, Christoph Scheytt, Heinz Nixdorf Institut/Universität Paderborn, Paderborn, Germany, MBMV, Virtuell, 18.-19.3.2021.
33. **Constrained Random Verification for RISC-V: Overview, Evaluation and Discussion** , Sallar Ahmadi-Pour1, Vladimir Herdt1;2, Rolf Drechsler1;2, 1Institute of Computer Science, University of Bremen, Germany, 2Cyber-Physical Systems, DFKI GmbH, Bremen, Germany, MBMV, Virtuell, 18.-19.3.2021.
34. **Towards RISC-V CSR Compliance Testing,** Niklas Bruns, Vladimir Herdt, Daniel Große, Senior Member, IEEE and Rolf Drechsler, Fellow, IEEE; IEEE EMBEDDED SYSTEMS LETTERS (ESL) journal, VOL. 13, NO. 1, MARCH 2021
35. **Towards Reliable Spatial Memory Safety for Embedded Software by Combining Checked C with Concolic Testing** , UB, DAC 2021, December 5-9, 2021, virtual
36. FZI plant ein Arbeitsergebnis aus Scale4Edge auf dem MBMV-Workshop im Rahmen einer live **Demonstration**, am 19.03.2021, zu präsentieren. Für die Veröffentlichung und zur besseren Einsichtnahme findet sich das Werkzeug auf GitHub: https://github.com/fzi-forschungszentrum-informatik/chips-core [7]. Hierbei handelt es sich um die **CHIPS (Chisel Hardware Property Specification) Sprache sowie unterstützendes Tooling**.
37. **New Techniques for the Automatic Identification of Uncontrollable Lines in a CPU Core** , Nikolaos I. Deligiannis[1], Riccardo Cantoro[1], Matthias Sauer[3], Bernd Becker[2], Matteo Sonza Reorda [1], [2] of Freiburg - Freiburg, Germany, [1]Politecnico di Torino, DAUIN - Torino, Italy, [3]Advantest - Böblingen, Germany, 26-28.4.2021, IEEE VTS 2021, Virtual
38. **µRV32: An Open Source RISC-V Cross-Level Platform for Education and Research** , Sallar Ahmadi-Pour[1], Vladimir Herdt [1,2], Rolf Drechsler[1,2], [1]University of Bremen, [2]DFKI GmbH Bremen, Germany, DESTION 2021, 18.5.2021.
39. Krishnamurthy, Pradeep, & Poppen, Frank. (2021, May 17). **Implementing VexRiscv Based Murax SoC on Arty A7 Artix-7 PCB from Digilent**

and Enabling JTAG Connection through Xilinx's BSCANE2 Debug IP. Zenodo. http://doi.org/10.5281/zenodo.4767195 [8]

40. **Adaptive Simulation with Virtual Prototypes in an Open-Source RISC-V Evaluation Platform** , Vladimir Herdt[1;2] Daniel Große[2;3] Sören Tempel[1] Rolf Drechsler[1;2], [1]Institute of Computer Science, University of Bremen, Bremen, Germany, [2]Cyber-Physical Systems, DFKI GmbH, Bremen, Germany, **3**Institute for Complex Systems, Johannes Kepler University Linz, Austria in Journal of Systems Architecture (JSA) [9], Elsvier, 2021
41. **Exploring Static Code Generation and SIMD-Acceleration for Machine Learning on RISC-V,** Rafael Stahl, Technical University of Munich, RISC-V Forum on "Developer Tools & Tool Chains", 2.6.2021
42. Johannes Müller, Mohammad R. Fadiheh, Anna Duque Anton, Thomas Eisenbarth, Dominik Stoffel, Wolfgang Kunz :" **A Formal Approach to Confidentiality Verification in SoCs at the Register Transfer Level**", *IEEE/ACM Design Automation Conference (DAC)*, Dec. 5-9, 2021, San Francisco/virtual, USA. (accepted)
43. **RISC-V AMS VP: An Open Source Evaluation Platform for Cyber-Physical Systems** , UB, FDL 2021
44. **In-Vivo Stack Overflow Detection and Stack Size Estimation for Low-End Multithreaded Operating Systems using Virtual Prototypes** , UB, FDL 2021
45. **Metamorphic Testing for Processor Verification: A RISC-V Case Study at the Instruction Level,** Frank Riese1 Vladimir Herdt1;2 Daniel Große3 Rolf Drechsler1;2 1Cyber-Physical Systems, DFKI GmbH, 28359 Bremen, Germany 2Institute of Computer Science, University of Bremen, 28359 Bremen, Germany 3Institute for Complex Systems, Johannes Kepler University Linz, Austria Frank [dot] Riese@dfki [dot] de, vherdt@uni-bremen [dot] de, daniel [dot] grosse@jku [dot] at, drechsler@uni-bremen [dot] de, UB, VLSI SoC 2021
46. **Automated HW/SW Co-design for Edge AI: State, Challenges and Steps Ahead** , Oliver Bringmann[1], Wolfgang Ecker[2], Ingo Feldner[3], Adrian Frischknecht[1],Christoph Gerum[1],Timo Hämäläinen[4], Muhammad Abdullah Hanif[5], Michael J. Klaiber[3], Daniel Mueller-Gritschneder[6], Paul Palomero Bernardo[1],Sebastian Prebeck[2], Muhammad Shafique[7]; [1] University of Tübingen, [2] Infineon Technologies AG, [3] Bosch Corporate Research, [4] Tampere University, [5] Technische Universität Wien, [6] Technical University of Munich, 7 New York University Abu Dhabi, Special Session, ESWEEK 2021, Virtual Conference, October 10 – 15, 2021
47. **Advanced Virtual Prototyping for Cyber-Physical Systems using RISC-V: Implementation, Verification and Challenges** ; Vladimir Herdt[1,2*] & Rolf Drechsler[1,2]; [1]Institute of Computer Science, University of Bremen, Bremen 28359, Germany; [2]Cyber-Physical Systems, DFKI GmbH, Bremen 28359, Germany, In Journal Science China Information Sciences (SCIS) - https://www.springer.com/journal/11432 [10], 2021
48. **Automated Detection of Spatial Memory Safety Violations for Constrained Devices** , Sören Tempel[1] Vladimir Herdt[1;2] Rolf Drechsler[1;2], [1]Institute of Computer Science, University of Bremen, Bremen, Germany, [2]Cyber-Physical Systems, DFKI GmbH, Bremen, Germany, ASP-DAC 2022

Das Projekt Scale4Edge wird unter den Förderkennzeichen 16ME0122K-16ME0140 im Förderprogramm ZuSE durch das deutsche Bundesministerium für Bildung und Forschung (BMBF) gefördert.

Links:
[1] https://www.hni.uni-paderborn.de/fileadmin/Publikationen/hni_aktuell/hni_aktuell_1_2020.pdf
[2] https://www.infineon.com/cms/de/about-infineon/press/press-releases/2020/INFXX202009-090.html
[3] http://dx.doi.org/10.1109/TCAD.2020.3012320
[4] https://tmt.knect365.com/risc-v-summit/
[5] https://doi.org/10.1145/3394885.3431584
[6] https://smarttampere.fi/en/home/
[7] https://github.com/fzi-forschungszentrum-informatik/chips-core
[8] http://doi.org/10.5281/zenodo.4767195
[9] https://www.journals.elsevier.com/journal-of-systems-architecture
[10] https://www.springer.com/journal/11432