

Yield as Fourth Design Target, the Challenge of Design for Yield

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Abstract

In the area of UDSM and today's continuously changing market conditions, yield ramp has become a key factor in driving product profitability. While product complexity is increasing the market windows are shrinking, a delay means decreased revenue as prices decline.

Painful ramping at the 130 nm node taught the industry a few important lessons:

Productivity advances in the future will come not only by feature shrinks, but also by new materials.

Yield ramping and final yields will not reach historical norms.

A key cause of not reaching previously attained yield levels is the gap between design and manufacturing.

For critical device features $< 0.25 \mu\text{m}$ the separation between design and manufacturing was not the main issue. Today as the industry is ramping 90 nm and developing 65 nm the design rules have become inadequate to describe the manufacturing reality and its impact on the design process. Also, the process variations definitely start becoming a nightmare for 65 and 45 nm devices.

As consequence of driving product profitability, yield as quality factor must be included as target besides area, performance and leakage during all stages of the design process. It turns out that a big time saving factor during ramp of a product is the early communication of design areas, that may be marginal in terms of design rules, defect density sensitivity etc., where metrology or inspections could focus on.

In the first part of the talk we address the need of introducing yield as fourth design target and its consequences for EDA tools. In the second part we concentrate on a proper Design for Yield & Manufacturability interface between the design and the manufacturing phase.

Curriculum Vitae



Bernd Lemaitre received the Diploma degree in Physics from Technical University Darmstadt, Germany at the Institute of Nuclear Physics and the PhD in Electronics from the University of Bundeswehr, Munich in 1992. In 1985 he joined Siemens AG, Semiconductor Division, now Infineon Technologies AG. As leader of a simulation group with the main interest in device modeling for enhanced CMOS technologies he worked in the area of CAD, technology development, device modeling and characterization. From 1998 to 2002 he held the position of a Vice

Chairman of the international Compact Model Council organized by the Electronic Industries Association (EIA). Since 2002 he is working in the area of Yield Management and Design for Manufacturing as a program manager for DfM at Infineon Technologies AG.



Uwe Gäbler received the Diploma degree in Electrical Engineering from Technical University Dresden, Germany in 1992. In 1992 he joined Fraunhofer Gesellschaft, Institute of Microelectronic Circuits and Systems Duisburg/Dresden, now IPMS Dresden. He worked in the area of circuit design, especially for digital and mixed-signal ASICs. From 1997 to 2001 he was working at Siemens HL, now Infineon, in the Product Engineering Department as Lead Engineer for quarter micron logic technology. From 2001 to 2003 he was working in the area of Design for Manufacturing, especially responsible for interaction between development and fabs. Since 2003 he is project leader of an Infineon project to speed up yield learning for sub-quarter micron technologies.

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