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Yield and Manufacturability: the 4th Dimension in Design Optimization

edaForum05 Presentation

Company Presentation

Magma Design Automation, Inc.

Yield and Manufacturability: the Fourth Dimension in Design Optimization

Abstract

Manufacturing process control has significantly improved, however, the relative weight of process variability is increasing, thus reducing the benefits expected from technology scaling. Methodologies are now needed to design robust circuits that do not rely on impossibly tight process control, as well as, to improve circuit manufacturability.

Post-layout processing such as RET and CMP-fill are already in use today to render circuits more manufacturable, however larger impact and faster turnaround time can be achieved if yield and manufacturability become the fourth dimension in the design optimization space. This approach brings manufacturability into the IC Design flow and requires an integrated design environment to enable the desired trade-off between all circuit metrics concurrently (timing, power, noise, area AND yield). This Manufacturing-Aware approach should address both functional and parametric yield loss and should complement existing postlayout verification and processing techniques.

To ensure high parametric yield, process and environmental variations have been traditionally taken into account by using conservative safety margins on top of a deterministic design flow. However, this approach is too conservative and is no longer feasible. Statistical timing analysis and optimization will be needed not only to provide a performance boost, but also to allow a more flexible performance/yield trade-off. In addition, to reduce functional yield loss, yield-driven approaches will be required, e.g. synthesis for yield and critical-area-driven wire optimization.

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