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Verisity Design Inc: Verification: Can't Live With It, Can't Live Without It

Company Presentation: Verisity Design, Inc.

Larry Lapides CVP Worldwide Sales & Product Operations Verisity Design, Inc. 

Abstract

In most companies, "verification" is the dirty little secret of engineering, the poor step-sister of design. Nobody wants to do verification, or if they do, they are put in an isolated cubicle and shunned by the rest of engineering. And managers want to assign the task, then assume it will get done.

The reality is, however, that to be successful with 90nm SoC designs verification must be embraced from the executive level on down. Verification is the Cinderella of the engineering team. Verification should be a core business practice, in the same way that Quality is a core business practice.

There are business implications to this: Verification should be a recognized engineering discipline, with a separate career path in the organization. There should be standard verification engineering practices and methods employed on all projects. Verification reuse becomes more important than design reuse. And with verification the key to success at 90nm and below, verification engineers should play a major role in the technical management of projects.

This presentation shows the challenges of verification for 90nm SoCs. A solution to these challenges, System Verification Process Automation (SVPA), is presented. SVPA includes the methodology required to verify from system specification to silicon, and this is discussed. SVPA also includes requirements for managing the verification task, and suggestions for overall business verification practices. Data from several case studies are presented in the areas of developing an organization with verification expertise, implementing verification reuse and managing the verification task.

edacentrum | Schneiderberg 32 | 30167 Hannover | fon: +49 511 762-19699 | fax:+49 511 762-19695 | emailinfo@
edacentrum [dot] denach oben

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