edaWorkshop09 and CATRENE DTC - Programm

Auf dieser Webseite finden Sie das Programm des edaWorkshop09 and CATRENE DTC, welches Sie für jede Session einzeln ausklappen können. Dort finden Sie den Zeitplan, die Vortragstitel sowie die Vortragenden. Wenn darüber hinaus noch Informationen wie eine Kurzfassung, ein Lebenslauf oder (für alle Teilnehmer) die Folien verfügbar sind, wird ein entsprechender Link unter dem Vortragstitel angezeigt.

Sie können das Programm auch als PDF-Datei herunterladen (591.17 K).

Dienstag, 26. Mai 2009

10:00 - 11:00
Welcome and Keynote
Moderator: Wolfgang Rosenstiel (edacentrum, D)

10:00	**Welcome** Helmut Bossy (BMBF)
10:15	**Keynote:** **System-level Design Technologies for Heterogeneous Distributed Systems** Giovanni De Micheli (EPFL) Kurzfassung und Curriculum Vitae

11:00 - 11:30
Coffee Break

11:30 - 13:00
Technical Session: System Level Design
Moderator: Frédéric Pétrot (TIMA/INPG)

11:30	**Integrated Analog-Digital HW/SW Co-Design** Nico Bannow (Bosch)
12:05	**Industrial Experience with System Level Design** Marcos Martínez (DS2)
12:30	**TSAR: Virtual Prototyping of a Scalable Multi-core Architecture** Alain Greiner (U Pierre & Marie Curie, Paris)
12:55	**Q&A**

13:00 - 14:00
Lunch

14:00 - 15:30
3D Integration Design & Technology
Moderator: Mario Diaz-Nava (ST Microelectronics, F)

14:00	**Potentials of 3D Integration Technology and Challenges for Design Support** Josef Weber (Fraunhofer-EMFT) Peter Schneider (Fraunhofer-IIS/EAS)
14:35	**3D Technologies and Data Structures – An Overview** Robert Fischbach (TU Dresden)
15:00	**CAD Tools and Design Flow for 3D Integration** Lisa McIlrath (R3 Logic)
15:25	**Q&A**

15:30 - 16:00
Coffee Break

16:00 - 17:30
LOMOSA/COMCAS Low Power Solutions
Moderator: Riccardo Locatelli (ST Microelectronics)

16:00	**A Power Aware Transactional Level Multiprocessor Soc Simulation Environment** Frédéric Pétrot (TIMA/INPG)
16:35	**Novel Method for Power Optimization in Cellular Baseband Circuits** Daniel Mueller (ST Ericsson)
17:00	**Power-Efficient Routing Implementation in Heterogeneous On-chip Networks** José Flich (TU Valencia)
17:25	**Q&A**

17:30 - 18:30
Panel
Moderator: Joseph Borel (JB R&D Consulting)

The purpose of the panel is to discuss the importance of an ESL concurrent design solution to develop better early optimized products versus present TSV designs using only a bottom up approach.

17:30	**TSV (Through Silicon Via) Technology as a Driver for ESL Design Solutions?** Asen Asenov (U Glasgow) Dominique Hénoff (ST Microelectronics) Riccardo Locatelli (ST Microelectronics) Peter Schneider (Fraunhofer-IIS/EAS) Geert Van der Plas (IMEC)

18:30 - 19:30
Break

19:30 - 23:00
Conference Dinner

19:30	**Meeting point at hotel reception**
19:45	**Arrival at "Italien Village"**
20:00	**Abendessen:** **Dinner**
23:00	**End of 1st day**

Mittwoch, 27. Mai 2009

09:00 - 09:45
Keynote
Moderator: Jürgen Haase (edacentrum, D)

09:00 **3D Integration for Multimedia Applications**
Dominique Hénoff (ST Microelectronics)
Kurzfassung und Curriculum Vitae

09:45 - 10:10
Coffee Break

10:10 - 11:45
Technical Session: Design and Verification of Analog/Mixed-Signal Circuits and Systems
Moderator: Ralf Popp (edacentrum, D)

10:10 **VeronA Paves the Way for Advanced Verification of Analog Circuits**
Peter Jores (Bosch)

10:40 **Joint Property Specification for Transient Simulation and Formal Verification of Analog Circuits**
Sebastian Steinhorst (U Frankfurt)

11:00 **SystemC-AMS for the Design of Complex Analog Mixed Signal SoC's**
Karsten Einwich (Fraunhofer-IIS/EAS)

11:20 **Modeling Heterogeneous Systems with SystemC-AMS: Application to Wireless Sensor Network**
François Pêcheux (U Pierre & Marie Curie, Paris)

11:40 **Q&A**

11:45 - 14:00
Poster Session
Moderator: Cordula Pröfrock (edacentrum)

11:45 **Introduction to the Poster Exhibition including the project "Synthesis-supported Design of Analog Circuits" (SyEnA)**

12:05 - 12:30
Poster Exhibition

Besides these reviewed contributions to edaWorkshop09, the poster exhibition will show posters and demonstrations of all EDA projects funded by BMBF within IKT 2020. Additionally all participants will have the possibility to contribute to the future updates of the multi-annual strategic plan (MASP) of the European research initiative ENIAC.

12:05 **Posterausstellung:**
A Rapid Prototyping Environment for ASIP Validation in Wireless Systems
Matthias Alles (TU Kaiserslautern)

12:05 **Posterausstellung:**
Fast Verification of A/MS-Systems for Automotive Applications
Rolando Dölling (Bosch)

12:05 **Posterausstellung:**
A Top-Down formal Verification Approach of LIN Hardware IP based on the GapFreeVerification(TM) Process
Oliver Sander (KIT)

12:05 **Posterausstellung:**
Multi-bit Error Detection for Self-Correcting CPU Pipelines
Abdelmajid Bouajila (TU Muenchen)

12:30 - 14:00
Lunch and Poster Exhibition

14:00 - 15:30
Technical Session: Design for Yield
Moderator: Georg Georgakos (Infineon)

14:00 **Yield Optimization and Assessment Methodologies in Physical Design**
Hanno Melzner (Infineon)

14:35 **Challenges in Analog Sizing for Yield and Reliability**
Helmut Gräb (TU München)

15:00 **Waveform-based Timing Analysis for Digital Circuits Using Current Source Models and Model Order Reduction**
Christoph Knoth (TU Muenchen)

15:25 **Q&A**

15:30 - 16:00
Coffee Break

16:00 - 17:30
Panel
Moderator: Herbert Rödig (Infineon)

16:00 **R&D Ecosystem to Build the European Electrical Car**
Carol de Vries (NXP)
Jochen Langheim (STMicroelectronics, F)
Bernd Ponick (U Hannover)
Christian Sebeke (Bosch)

17:30 - 18:00
Break

18:00 - 23:00
Social Event

18:00 **Meeting point at hotel reception for guided tour**
Christian Sebeke (Bosch)

18:15 **Guided tour at "VW Transparent Factory"**

19:00 **Meeting point at hotel reception**

19:15 **Arrival at "Lesage"**

19:30 **Social Event:**
Award of "EDA-Medaille 2009"
Weitere Informationen

19:45 **Abendessen:**
Dinner

23:00 **End of 2nd day**

Donnerstag, 28. Mai 2009

09:00 - 09:45
Keynote
Moderator: Norbert Wehn (TU Kaiserslautern)

09:00 **Function-oriented Development**
Klaus Revermann (VW)
Kurzfassung und Curriculum Vitae

09:45 - 11:10
Autonomous Integrated Systems
Moderator: Volker Schöber (edacentrum)

09:45 **Reliability and Safety-Guarantees in Modern MPSoCs with Real-Time Requirements**
Maurice Sebastian (TU Braunschweig)

10:10 **ESL Power Estimation for Embedded Processors**
Björn Sander (FZI)

10:35 **A Demonstration Platform for Autonomous Integrated Systems**
Norbert Wehn (TU Kaiserslautern)

11:10 - 13:00
Coffee Break

11:10 - 13:00
Poster Exhibition

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Matthias Alles (TU Kaiserslautern)

13:00 - 14:30
Lunch

14:30 - 16:05
Test, Reliability and Validation
Moderator: Erich Barke (edacentrum)

14:30 **MAYA - A Significant Step for Efficient Production Testing and Faster Yield Learning**
Jürgen Alt (Infineon)

15:00 **Fault-tolerant Interconnects Using Codes and Self-repair**
Daniel Scheit (TU Cottbus)

15:30 **A Rapid Prototyping Environment for ASIP Validation in Wireless Systems**
Matthias Alles (TU Kaiserslautern)

15:55 **Closing words**
Erich Barke (edacentrum)

16:05 **End of 3rd day**

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