Transaction Level Modelling in SystemC

Technical Session 2

The 7th Heaven of System Level Design

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Abstract

This talk will describe the Transaction Levels of modeling within SystemC. The various abstraction levels within Transaction Level Modeling (TLM) are identified, and the overview of the APIs is given. Three main TLM levels will be defined: Programmers View (PV), Programmers View plus Timing (PVT) and Cycle Callable (CC). Programmers View captures the behavior of the hardware components, as seen by the embedded software developer. The model is bit-true, register accurate, no clock, no timing, enough synchronization to enable correct functionality. Transactions at this level represent information which may be passed over a number of cycles. The interface is blocking and reactive. Programmers View plus Timing inherits the PV model and includes timing and other benchmarking or debugging information. Additionally, there is synchronization with the system clock. In all other ways, it is identical to the PV. Cycle Callable is clocked, can use abstract data types, and is statically schedulable. Data is transferred by polling, not by reactive function calls. Transactions at this level represent the information passed in one cycle. Each module is refined to model the cycle behavior of the IP (pipelining, communication protocols and structures, out-of-order computations, split responses, etc.). The talk will give some details of ARM's proposed implementation of these levels and how they fit into a design flow.

Curriculum Vitae

Mark Burton gained a BEng in Computer Systems Engineering from Warwick University and his PhD from Leeds University. Since then he has worked at Inmos implementing the ALU for the T9000 Microprocessor. At ACRI he designed and implemented the modeling and validation strategy. While at ARM, Mark has been responsible for implementing a number of innovative modeling strategies. He is now the engineering manager responsible for ARM's Models and Modeling Technologies. Mark is also the chair of the OSCI SystemC Transaction Level Modeling Group, which is currently defining how modeling should be done across a number of abstraction levels. ARM's Modeling group’s mission is to be the global center of excellence in terms of both models, and their application to a design flow.