The TETRISC SoC for safety critical applications

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Abstract

To promote the advancement of RISC-V-processors into the safety-critical domain, we focus our investigations on reliability and resiliency. In this context, our main target is the development of a highly reliable pulpissimo-based multiprocessor platform with fault tolerance mechanisms on circuit, core and system level, resulting in a robust multiprocessor SoC that is suitable for harsh environments. In order to achieve this, we hardened certain cells, added shadow registers and quadrupled the RI5CY core, thereby forming the TETRISC SoC (TETra Core System based on RISC5). The complementary HiRel Framework Controller, which acts as an in- and output multiplexer and voter, enables the forming of different NMR subsystems between the cores. Based on the harshness of the environment extracted from radiation, temperature and ageing sensors, the system is thus able to switch between high performance, DMR, TMR or QMR mode, without interrupting the computation of the non-included cores.

Biography

Dr. Markus Ulbricht received his doctorate degree from Brandenburg University Cottbus-Senftenberg in 2014 on the topic of ”Systematic lifetime-optimization of highly integrated systems on the basis of nano-structures by means of stress optimization and self repair”. In the following two years he collected thorough experience as a test engineer at Intel Communications GmbH in Munich. To have a stronger focus on his scientific career, he transferred to IHP in 2016, where his first projects involved backend HDL design and the design and implementation of a fault tolerant radar platform for distance measurements for automated driving. As of 2020, he is leading the fault tolerant computing group with a strong focus on sensory platforms and open source hardware as well as reliable computing and neuromorphic processing systems.