Talk 2: Towards Trustworthy RISC-V Processors for Safety-critical Applications

Salaheddin Hetalani, Siemens EDA, DE

Abstract

RISC-V is one of the hottest trends in the industry these days, with its mature software toolchain and many hardware processor providers offering implementations ranging from textbook open-source cores to high-end commercial ones. The freedom to configure and customize the RISC-V ISA in accordance to the system needs, including custom instructions, is one of its strongest appeals, making custom RISC-V CPUs an attractive choice for an unprecedented number of companies. However, the challenge of actually designing a RISC-V core with custom extensions and ensuring its correct functional behaviour is still significant, even more in environments with high safety and security expectations. In this session, we present an automated flow to generate RISC-V cores with custom extensions together with their complete verification.

Biography

 Salaheddin Hetalani holds a M. Sc. in Embedded Computing Systems as a joint degree from the Technical University of Kaiserslautern and Southampton University and has around 3-year experience in formal design verification. He is working at Siemens EDA as Field Application Engineer and focuses on application and development of RISC-V and bus protocol VIPs