SystemVerilog at the Transaction Level

Technical Session 2

The 7th Heaven of System Level Design

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Abstract

There is a need to design and verify systems at an abstraction level which reflects some of the architecture and performance of the system under design, without too much detail. The communication between subsystems is usually modeled as transactions.

The traditional hardware description languages, Verilog and VHDL, do not support transaction level models well because they lack all the necessary constructs. Hardware verification languages lack the structural modeling constructs needed to represent the architecture. Programming languages lack the low-level hardware support needed to complete the design flow.

SystemVerilog combines the features of a hardware description language and a hardware verification language, and supports the design and verification of systems at the transaction level. The flexibility of interfacing to C allows the integration of processor models to simulate embedded software. The combination allows a high performance verification of the system architecture.

Curriculum Vitae

Peter Flake was a founder and Chief Technical Officer at Co-Design Automation and was the main architect of the SUPERLOG language. His EDA career spans 30 years: he was the language architect and project leader of the HILO development effort while at Brunel University in Uxbridge, U.K., and at GenRad. HILO was the first commercial HDL-based simulation, fault simulation and timing analysis system of the early/mid 1980s. With the acquisition, Peter Flake became a Scientist at Synopsys.

He holds a Master of Arts degree from Cambridge University in the U.K. and has made many conference presentations on the subject of HDLs. He served on the Accellera SystemVerilog committees from their inception.