STRV – A SEU tolerant RISC-V implementation

Alexander Walsemann, University of Applied Sciences Dortmund, D

Abstract

The STRV is a RV32-IMC RISC-V core with integrated protection against Single-Event-Upsets (SEUs). It uses triple modular redundancy (TMR) and majority voting to automatically detect and correct encountered SEUs within the core and memory. The error detection and correction is done exclusively at the hardware level. Therefore, no modifications to the executed software are required to utilize the protection against SEUs. Additional memory-mapped registers are available to get information about the number of encountered SEUs. The current implementation is a reference design that will be used for comparative studies with future designs and to evaluate the relationship between power consumption, size and redundancy. The STRV was developed for use in experimental laboratories conducting research in the field of high-energy physics. However, it could also be used in other fields exposed to ionizing radiation. First silicon is expected to arrive for initial testing in November 2021.

Biography

 Alexander Walsemann received the B.Eng. and M.Eng. degrees in electrical engineering from University of Applied Sciences Dortmund, in 2017 and 2019, respectively. He is currently pursuing the doctoral degree (Ph.D.) at the department of Automation / Computer Science, University of Wuppertal. He has been involved in the development of custom ASICs for high-energy physics experiments since 2017. His current research interests include microprocessor architecture, radiation-tolerant design, and low-power optimization.