Sometimes the Answer is Outside the Box

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Abstract

The market and technical pressures of IC design today are forcing engineers away from ASIC-based projects, and forcing them to consider other logic alternatives. ASIC design times are longer than ever experienced, particularly when targeting silicon below 100 nm technology densities. More complex timing prediction, expensive parasitic extraction and analysis tools, new tool training, exorbitant mask costs, and the time and cost of verification in sub-micron ASIC designs now dominate the design flow. But there is a clear alternative available to let you avoid all of this confusion and cost, increase your productivity and at the same time reduce your risk, it is FPGA programmable logic design.

Programmable FPGA-based design methodologies let you increase productivity and lower design costs by removing the silicon design and verification headaches; moving your design freeze much farther out, even after product delivery. FPGA design tools offer added performance advantages with mature tool flows that help ASIC-to-FPGA design conversion with analysis, formal verification, and real-time debug technology that can slash up to 50% off your verification cycle. Advanced optional technology like RT-level floorplanning, FPGA physical synthesis, incremental design, and modular design tailor FPGA implementation tools to your specific corporate design environment, increase design performance, and shorten the design cycle, particularly for high-density designs.

Curriculum Vitae

Giles Peckham has worked on the silicon side of IC design for over twenty years, covering the whole spectrum from full custom SoC designs through Standard Cells, Gate Arrays and now Programmable Logic. He currently works for Xilinx where he is responsible for marketing Xilinx‘ product and services solutions in Europe. His experience in design and field applications roles supports his special interest in the advanced EDA flows used for today‘s high density and high performance FPGAs.