

# RISC-V Models for Verification, Software Development and Architectural Exploration

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## Abstract

As RISC-V processors start to be used more and more in SoCs, industry needs to look beyond the RISC-V ISA to the requirements for use. These include a well-verified implementation, the ability to develop, debug and test software, especially early in the project, and the need to explore different implementations, including different processors, multi-hart processors and custom instructions. One common element to these requirements is a high quality model of the RISC-V cores being used. This presentation will report on the test driven development methodology used to build the Open Virtual Platforms (OVP) models of RISC-V cores (~50 different cores available in the OVP Library and provided to processor IP developers), and show how these models have been used for design verification, software development and architectural exploration.

## Biography



Larry is currently VP Worldwide Sales at Imperas Software Ltd., and previously ran worldwide sales at EDA companies Averant and Calypto Design Systems. He was vice president of worldwide sales during the run-up to Verisity's IPO (the top performing IPO of 2001 in the U.S.), and afterwards as Verisity solidified its position as the fifth largest EDA company. Before Verisity and SureFire Verification (acquired by Verisity), Larry held positions in sales and marketing for Exemplar Logic and Mentor Graphics. Prior to moving into marketing and sales, Larry spent 9 years working on infrared photodiode design and fabrication.

Larry has been on the Clark University Graduate School of Management (GSOM) Advisory Council since 2003, and was an Entrepreneur-in-Residence at Clark during Fall 2006, when he developed and taught the course on Entrepreneurial Communication and Influence.

Larry holds a BA in Physics from the University of California Berkeley, a MS in Applied and Engineering Physics from Cornell University and a MBA from Clark University.