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A RISC-V based Edge Computing Platform with Interchangeable Cores Using 22FDX

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Abstract

In this talk, we will present a configurable, low-power edge computing platform for efficient sensor signal processing. The platform is composed of a RISC-V processor core, a hardware accelerator, and a distributed memory architecture with dynamic content re-allocation. Following a strict hardware/model co-design approach, we have derived an optimized low-power hardware accelerator for temporal convolutional networks using a configurable array of processing elements with optimized access to the distributed memory architecture. We have integrated different RISC-V processor cores into our edge computing platform and will present the results of two alternative core implementations in Globalfoundries' 22FDX technology.

Biography

 Paul Palomero Bernardo was born in Tübingen, Germany, 1996. He received the B.S. and M.S. degrees in computer science from University of Tübingen, Tübingen, Germany, in 2017 and 2020, respectively, where he is currently pursuing the doctoral degree (Ph.D.) at the Department of Computer Science. His current research interests include neural network hardware and design optimization.