The Next Big Advance in Chip-Level Design Productivity

Richard A. Newton, Dean of the College of EngineeringUniversity of California, Berkeley

Abstract

In the mid-1980's, the design technology industry made its last major advance in design productivity with the introduction of a logic-synthesis-based design methodology and associated verification techniques, built largely as an extension of the existing logic-level library-based ASIC industry. Since then, we have extended the range (and lifetime) of that approach somewhat, with the introduction of "RTL-level design" and "IP reuse" for example, while many of us have worked to understand what will be the next mainstream major shift in single-chip silicon design methodology. It is important to observe that every major improvement in design productivity has been led by a significant step in design methodology and associated verification strategies. Over the past fifteen years we have proposed "hardware-software codesign" and have developed complex chips (especially DSP's) with special-purpose hardware for virtually any application mix. We have proposed and developed dynamically-programmed FPGA-based approaches, VLIW and super-scalar architectures, SIMD and a plethora of other hardware and software variations, even declaring the "end of ASICS" and a solid future for application or task-specific processors. Through my role as Director of the GSRC, and my exposure to Silicon Valley and its many start-ups, I have had the opportunity to study all of these approaches. After many years, I finally believe I know the answer to the question "What will be the next big advance in single-chip design productivity?" and I will describe it in this presentation!

Curriculum Vitae

Richard Newton is currently Dean of the College of Engineering and the Roy W. Carlson Professor of Engineering at the University of California, Berkeley. He has been a Professor in the Department of Electrical Engineering and Computer Sciences at Berkeley since 1979, where he has been actively involved as a teacher and researcher in the areas of design technology, electronic system architecture, and integrated circuit design. Over the past twenty years, he has received a number of awards for his research and he was selected in 1987 as the national recipient of the C. Holmes McDonald Outstanding Young Professor Award of the Eta-Kappa-Nu Engineering Honor Society in recognition of his teaching.

From 1998-2002, he was the founding director of the MARCO/DARPA Gigascale Silicon Research Center (GSRC) for Design and Test. An industry-university-government research collaboration with an annual budget of US$8M, the GSRC coordinates the research of more than thirty faculty, eighty graduate students, a dozen postdoctoral researchers, and many industrial collaborators to tackle some of the design and test problems for integrated silicon systems that will face chip designers 6-12 years from now.

In addition to his academic role, Professor Newton has helped to found a number of design technology companies, including SDA Systems (now Cadence Design Systems), Simplex Solutions, Tensilica, Crossbow, and Synopsys, where he has rejoined the Board of Directors. Since 1997, he has also been a member of the Technical Advisory Board of the Microsoft Research Laboratories.

Since 1988, he has served as a Venture Partner with the Mayfield Fund, a high-technology venture capital partnership, where he has contributed to both the evaluation and early-stage development of over two dozen new companies, including Silicon Light Machines, now a part of Cypress Semiconductor, and where he was the acting President and CEO during 1994 and 1995.

He is a member of the ACM and a Fellow of the IEEE.

edacentrum | Schneiderberg 32 | 30167 Hannover | fon: +49 511 762-19699 | fax:+49 511 762-19695 | email info edacentrum [dot] denach oben

---