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[Startseite](#) > Druckeroptimiertes PDF

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# Keynote: Gaining 10x in Power Efficiency in the Next Decade in Consumer Products

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## Abstract

Analog/RF design is becoming digital, through accurate CAD modeling of RF effects, and compensation in digital. At the same time, nergy-efficient Digital is becoming Analog, thanks to elaborate CAD-enabled design techniques like well-biasing, power-switches, over-/under-voltage, etc. In Analog/RF, improving the energy efficiency of consumer systems will be based on sensing continuously the system environment and tailoring the emitted power dynamically. Similarly in Digital, very-fine-grain closed-loop Dynamic-Voltage-Frequency-Scaling (DVFS) will enable to consume power only when and where required. Concurrently, heterogeneous co-design CAD methods will allow a holistic approach to energy efficiency, taking into consideration not only the IC with its system design architecture, but also its packaging and power source, and possibly the antenna.

Finally, a tailored advanced CMOS process will provide tuned transistors and passive components to enable the digital and analog design solutions needed, in conjunction with TSVs enabling optimized heterogeneous 3D stacking capabilities. A new generation of EDA tools, providing a holistic view of the system, will enable the complete system optimization and a 10x power efficiency gain.

In Europe, the Grenoble-Dresden Clusters are uniquely positioned to address the above challenges with a complete set of worldclass industrial and academic research facilities in advanced CMOS, 3D-stacking, design, system architectures and EDA.

## Curriculum Vitae



Gerd Teepe is director of Dresden Design Enablement of GLOBALFOUNDRIES. He graduated from the RWTH Aachen University (Dipl. 1982, PhD. 1986). He then worked on fault tolerant microprocessors at the NEC-Central-Research-Laboratories, Tokyo, Japan. For Motorola-Semiconductors in Europe, Teepe held various engineering and management positions in design, marketing and product-operations. Gerd Teepe joined AMD in Dresden in 2004 and is part of GLOBALFOUNDRIES since its foundation in 2009.



Philippe Magarshack is Technology Group Vice-President and Central CAD & Design Solutions General Manager at STMicroelectronics in Crolles, France. He started his career at AT&T Bell Labs in Murray Hill, NJ, in 1984, as a designer for the first 32bit microprocessor family. In 1989 in joined Thomson-CSF in Grenoble, and in 1994, he joined the Central R&D group at STMicroelectronics in Crolles. Magarshack now oversees ST's EDA and libraries strategy, enabling products in advanced CMOS and derivatives, and Smart Power.

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