Keeping Hot Chips Cool

edaForum05 Presentation

Technical Session I

Ruchir Puri, IBM Keeping Hot Chips Cool

Abstract

With 90 nm CMOS in production and 65 nm testing in progress, power has been pushed to the forefront of design metrics. Exponential increase in sub-threshold and gate leakage power is slowing down CMOS scaling. In addition, due to increasing variability in sub-90nm process, the variability in power dissipation has been a source of dropping yields, i.e., a significant portion of the yield is now power-limited in high-performance designs. In order to continue the CMOS scaling, it is crucial to tame this exponential increase in power dissipation. This talk will outline practical techniques that are used to reduce both leakage as well as active power in a standard-cell library based high-performance design flow. It will be about the design and cost issues for using different power saving techniques such as: power gating to reduce leakage, multiple and hybrid threshold libraries for leakage reduction and multiple supply voltage based design.

In addition, techniques to reduce clock tree power will be presented as power consumed in clocks accounts for a significant portion of total chip power. Practical aspects of implementing these techniques in high-performance designs will be stressed.

Biography

Ruchir Puri Manager, Logic & Physical Synthesis IBM Thomas J. Watson Research Center

He received M. Tech. degree in electrical engineering from Indian Institute of Technology (IIT), Kanpur, India in 1990, and a Ph.D. degree in electrical and computer engineering from University of Alberta, Canada in 1994. From 1994 to 1995 he was a Member of Scientific Staff with Advanced System Design Tools group at NORTEL Research (BNR). He joined VLSI Design Automation group at IBM in 1995, where he is a Research Staff Member and Manager of Physical and Logic Synthesis research group. He has been working on design and automated synthesis solutions for IBM s products and has received several IBM awards for his work. He has also been an adjunct assistant professor in the Department of Electrical Engineering at Columbia University, New York where he taught VLSI design and Circuits. He is inventor of 14 U.S. patents and has authored over 70 publications on the design and synthesis of low-power and high-performance circuits.