# Globally Optimized Robust System Design

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## Abstract:

Future system design methodologies must accept the fact that the underlying hardware will be imperfect, and enable design of robust systems that are resilient to such imperfections. This talk will describe enabling tools and technologies for building such systems. This presentation is about three techniques that can enable a sea change in robust system design:

1. Built-In Soft Error Resilience (BISER) 2. Circuit Failure Prediction 3. Concurrent Autonomous Self-Test and Self-Diagnosis

These techniques span multiple abstraction layers (circuit, architecture, virtualization and application), and enable global optimization across these layers. The applicability of robust system design techniques in overcoming the growing challenge of post-Silicon validation will also be discussed.

## Curriculum Vitae

 Dr. Subhasish Mitra is an Assistant Professor in the Departments of Electrical Engineering and Computer Science of Stanford University. His research interests include robust system design, VLSI design, CAD and test, and design for emerging nanotechnologies. Prior to joining Stanford, he was a Principal Engineer at Intel. He received Ph.D. in EE from Stanford. Dr. Mitra has co-authored more than 100 technical papers, and his robust system design techniques have seen wide-spread proliferation. His X-Compact technique for test compression is used by more than 50 Intel products, and is supported by major CAD tools. His work on imperfection-immune circuits using carbon nanotubes, jointly with his students and collaborators, has been highlighted as a "significant breakthrough" by the Semiconductor Research Corporation, MIT Technology Review, EE Times, and many others. His major honours include the NSF CAREER Award, Terman Fellowship, IEEE TCAD and DAC Best Paper Awards, ACM SIGDA Outstanding New Faculty Award, Intel Divisional Recognition Award and the Intel Achievement Award, Intel's highest corporate honour, "for a breakthrough test compression technology."