Full Programe - University Booth at DATE 2008

Tuesday, March 11, 2008

10:00 - 12:00	Session	Test, Yield and Costs		UB 1.1
University of Limerick	Ian Grout	CMOS Implementation for Data Converter BIST/BOST	Two silicon implementations for BIST and BOST solutions for data converter self-test are to be demonstrated. In these solutions, self-test functions for 16-18 bit data converter designs are undertaken with communications to an external PC. The systems provide the capability for on-chip or on-DIB signal generation, data capture and communications.	**1**
University of Siegen	Michael Wahl	Design Cost Controlling	CostMoS-G is a tool for collaborative work on cost optimal designs. The user can define arbitrary cost models for the products life cycle. Users are designers, managers, and controllers. Monte-Carlo simulation allows dealing with value ranges, and the integrated time model permits cost predictions for future reviews.	**2**
University of Bremen	Christian Genz	A graphical SystemC refinement tool	We present a graphical design tool that supports the manual refinement of SystemC models with focus on the following features. Separation of HW/SW partitions encapsulated in distinct hierarchies. Highlighting of synthesizable and non-synthesizable fragments of the design.	**3**
University of Bremen	Kishore Duganapalli	GA based ATPG Tool for Crosstalk Induced Logic Faults between On-chip Aggressor and Victim	The ATPG tool proposed here based on Genetic Algorithm, reads the circuit description and generates test patterns for the given set of aggressors and victims in DSM chips.	**4**
University of Bremen	Shehzad Hasan	Test Compaction of Crosstalk Faults through Fault List Reordering	Crosstalk noise may cause undesirable effects including excessive overshoot, undershoot, glitches, additional signal delay as well as signal speed-up. An algorithm is proposed for generating test patterns that produce maximal crosstalk effect on any interconnect of a circuit using existing ATPG tool and coupling influence between interconnects. The fault list is then reordered so as to reduce the total number of test patterns.	**5**

12:00 - 14:00	Session	Bringing Ideas into FPGAs		UB 1.2
Technical University of Braunschweig	Henning Sahlbach, Sean Whitty	FlexFilm: Real-time digital film processing with a FPGA-based reconfigurable platform	The FlexFilm board is a reconfigurable platform based on four Virtex II Pro FPGAs. Several run-time reconfigurable algorithms for real-time digital film processing for resolutions up to 2048x1556 pixels@24 FPS in 10-Bit RGB are demonstrated. The system achieves a sustained performance of 170 GOPS.	**1**
Ulm University	Frank Slomka	Submarine Explorer – A low cost AUV	The demonstrator is a low cost autonomous underwater robot. The computer system controlling the robot is design using advanced hardware/software codesign techniques by using state of the art FPGA SOPC technology implementing time critical parts of the system in hardware and using parallel computational resources by a consequent MPSOC approach. Using just one design environment a distributed embedded real-time system is presented. The system contains 4 FPGA boards connected by CAN and Ethernet links.	**2**
University of Erlangen-Nuremberg	Dmitrij Kissler	A High-Speed Dynamic Reconfigurable Multilevel Parallel Architecture	The CoMap project investigates the holistic co-design of a new class of highly parameterizable, massively parallel processor architectures. This architecture type is called weakly programmable processor arrays (WPPAs). Two DSP algorithms were implemented with the help of dynamic reconfiguration on the same WPPA hardware, prototyped on FPGA.	**3**
University of Pisa	Luca Fanucci	SHINE: FPGA prototyping of SpaceWire IP cores for High Data Rate and Fault Tolerant Invehicle Networking	An FPGA, hosted by a Nallatech BenNUEY PCI-board, is programmed with an 8-port SpaceWire Router IP core featuring an AMBA AHB interface. The router is controlled by a PC through a PCI/AHB bridge. A user-friendly GUI, which hides a dedicated software layer, provides full control over router features (link speed, router table, etc.) and monitors relevant traffic information.	**4**
Eindhoven University of Technology	Akash Kumar	PreMaDonna: Predictable Matching of Demands on Networked Architectures	We demonstrate a methodology to generate multiprocessor systems-on-chip from the high-level description of applications, namely synchronous dataflow graphs. An automated framework is presented to generate system-level designs for Xilinx FPGAs in seconds. Attendees will get an opportunity to experiment with this framework and generate multi-processor designs.	**5**

14:00 - 16:00	Session	System Exploration and Transaction Level Modelling		UB 1.3
RWTH Aachen University	Torsten Kempf	An ESL Workbench for early MPSoC Design Space Exploration	One major issue in future MPSoC designs is the combined hardware and software development, often referred to HW/SW co-design. Here, both hardware and software are developed in parallel manner, imposing new design challenges to the system architects.To cope with this issue during MPSoC design we have proposed a higher abstraction level, where an abstract processor simulator called Virtual Processing Unit (VPU) is utilized.	**1**

University of Tehran	Mahshid Sedghi	TLM Synthesis Studio	TLM Synthesis Studio is an environment to help system level designers start the design and implementation of their systems from transaction level. It supports OSCI TLM library and SystemC. It also provides the designers with a library of configurable TLM components.	**2**
Université de Bretagne Sud	Johann Laurent	SoftExplorer	SoftExplorer is a power/energy estimation tool that is developed into the Low Power Design Group of the LESTER laboratory. This tool allows the programmer to rapidly estimate the power and energy consumption of its application executed (for example a C code) on a processor (for example a TI TMS320C62). SoftExplorer owns several power models of processors.	**3**
Osaka University	Ittetsu Taniguchi	SoC Architecture Explorer	Architecture design in IP-based design is difficult because of vast design space. SoC Architecture Explorer explores the design space automatically and a number of architectures are output, which have a trade-off relation between performance and hardware area.	**4**
Université de Bretagne Sud	Pierre Bomel	A lightweight and remote partially reconfigurable platform	We present the concept of a networked lightweight and partially reconfigurable platform assisted by a remote bitstreams server. We propose a software and hardware architecture as well as a new data-link level network protocol implementation dedicated to dynamic and partial reconfiguration of FPGAs. These systems target embedded applications with very scarce hardware resources taking advantage of dynamic, specific and optimized architectures.	**5**
Université de Bretagne Sud	Philippe Coussy	GAUT – A High-Level Synthesis tool for DSP applications	Starting from a pure C function GAUT generates a potentially pipelined architecture composed of a processing unit, a memory unit, a communication unit with a GALS/LIS interface. The synthesis constraints are the data average throughput, the clock frequency, the FPGA/ASIC target technology and optionally the memory architecture/mapping, the I/O timing diagram. GAUT generates an IEEE-P1076 VHDL file and test benches which is an input for commercial logical synthesis tools like ISE/Foundation from Xilinx, Quartus from Altera or DC from Synopsys.	**6**
KU Leuven	Andy Lambrechts	The Coffee framework: COmpiler Framework for Energy-aware Exploration	Modern mobile devices need to be extremely energy efficient. This demo presents a unified optimization and exploration framework, from source level transformation to processor architecture design. The retargetable compiler and simulator framework can map applications to a range of processors and memory configurations, simulate and report detailed performance and energy estimates. An accurate energy modeling approach is used which can help to guide the design process.	**7**

16:00 - 18:00	**Session**	**Software and Hardware in the System**	**UB 1.4**

Université de Bretagne Sud	Rachid Dafali	µSPIDER CAD TOOL: CASE STUDY OF NOC IP GENERATION FOR FPGA	This demo presents the µSpider CAD tool for network on chip design under latency and bandwidth constraints and described the different steps of the associated design flow. We show: 1) how the tool can be used to automatically generate a NoC IP compliant with Xilinx EDK tool and 2) a real case implementation of a video application running on a Virtex2pro FPGA, the architecture includes 2 Mblaze, 1 PPC and our NoC IP.	**1**
Université de Bretagne Sud	Pierre Bomel	A mixed (hardware and software) rapid prototyping platform.	PALMYRE is set of hardware components and software tools enabling the rapid prototyping of telecom-oriented application. DSPs from Texas Instruments and FPGAs from Xilinx can be freely mixed to build a specific computing and communication topology. The demonstration is a pipeline of two DSPs and an FPGA Viterbi decoder. Thanks to the GALS/LIS approach the system is data regulated and can be stopped and restarted without loss of any data or synchronization between DSPs and FPGA.	**2**
Eindhoven University of Technology	Andreas Hansson	CoMPSoC - A Composable and Predictable Multi-Processor System-on-Chip Template	We propose a Composable and Predictable Multi-Processor System-on-Chip (CoMPSoC) platform and mapping methodology. Multiple real-time jobs can run simultaneously. Incremental integration and platform virtualisation are supported. The real-time jobs are analysed and verified independent of one another, using state-of-the-art dataflow techniques.	**3**
University of Paderborn	Christopher Pohl	Hardware-in-the-Loop Simulations with Matlab/Simulink/ModelSim for FPGA based designflows	This demonstrator shows the design flow and a working example of our Hardware-in-the-Loop Design Environment for FPGAs. Arbitrary VHDL designs can be automatically integrated into simulation or visualization tools, enabling functional verification and real time monitoring of that hardware design.	**4**
University of Paderborn	Thorsten Jungeblut	General Purpose VLIW Processor for Multiband-Multistandard applications	This demonstrator proposes our General Purpose VLIW-Processor for applications on mobile phones. Four arithmetic logical units can process scalar or SIMD instructions in parallel. The system is designed for 300 Mhz and achieves a performance of 1.2 GIPS or 2.4 VOPS.	**5**
Darmstadt University of Technology	Kurt Ackermann	Demonstration of a Self-Reconfigurable Video-Processing Frame-grabber	Limitations of logic and RAM resources of FPGAs are bottlenecks for many complex algorithms. Modern FPGAs support dynamic reconfiguration. Partitioning of complex algorithms in smaller sequentially reconfigured and executed units makes smaller FPGA devices suitable. A video processing framegrabber, connected to a high resolution matrix camera, is implemented as a demonstrator for a complex self-reconfigurable design on a Virtex-4 based evaluation board.	**6**

Wednesday, March 12, 2008

10:00 - 12:00	**Session**	**Mixed Signal Design, Test Solutions and More**	**UB 2.1**

Fraunhofer-Institut für Techno- und Wirtschaftsmathematik	Jochen Broz	Behavioral Modeling using Analog Insydes	Analog Insydes is a tool for modelling and analyzing analog circuits symbolically. For handling model complexity, it provides the methodology of symbolic approximation which is an innovative model-order reduction technique. The process works under full error control and allows the user to specify tolerance margins for the accuracy of the generated model.	**1**
University of Limerick	Ian Grout	CMOS Implementation for Data Converter BIST/BOST	Two silicon implementations for BIST and BOST solutions for data converter self-test are to be demonstrated. In these solutions, self-test functions for 16-18 bit data converter designs are undertaken with communications to an external PC. The systems provide the capability for on-chip or on-DIB signal generation, data capture and communications.	**2**
RWTH Aachen University	Torsten Kempf	An ESL Workbench for early MPSoC Design Space Exploration	One major issue in future MPSoC designs is the combined hardware and software development, often referred to HW/SW co-design. Here, both hardware and software are developed in parallel manner, imposing new design challenges to the system architects.To cope with this issue during MPSoC design we have proposed a higher abstraction level, where an abstract processor simulator called Virtual Processing Unit (VPU) is utilized.	**3**
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University of Southampton	Reuben Wilcock	Post Manufacture Variability Improvement Using Configurable Analogue Transistors (CATs)	Analogue design is becoming a bottleneck in DSM chips due to increased process variability. A configurable analogue transistor (CAT) structure is proposed which allows post manufacture adjustment of critical devices. The demonstrator shows live results from a silicon prototype, highlighting the adjustability and improvement offered by this approach.	**6**
12:00 - 14:00	**Session**	**System Analysis, Simulation and Verification**		**UB 2.2**
University of Bremen	Christian Genz	A graphical SystemC refinement tool	We present a graphical design tool that supports the manual refinement of SystemC models with focus on the following features. Separation of HW/SW partitions encapsulated in distinct hierarchies. Highlighting of synthesizable and non-synthesizable fragments of the design.	**1**

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University of Tokyo	Yoshihisa Kojima	A verification environment for high-level designs based on system dependence graphs	This tool provides a verification environment for high-level design descriptions. Program slicing, static code checking, dynamic simulation and formal equivalence checking based on symbolic simulation are realized on top of our ExSDGs (system dependence graphs integrated with abstract syntax trees).	**4**
University of Newcastle upon Tyne	Andrey Mokhov	Workcraft: a static data flow structure editing, visualisation and analysis tool	Reliable high-level modelling constructs are crucial to the design of efficient asynchronous circuits. Workcraft is a tool which aims to provide a common, cross-platform environment. The tool offers a GUI-based framework for visual editing, real-time simulation, animation and extendable analysis features for different SDFS types. The models themselves, as well as the supporting tools, are implemented as plug-ins.	**5**
14:00 - 16:00	**Session**	**SoC, Platforms and SystemC**		**UB 2.3**
University of Tehran	Mahshid Sedghi	TLM Synthesis Studio	TLM Synthesis Studio is an environment to help system level designers start the design and implementation of their systems from transaction level. It supports OSCI TLM library and SystemC. It also provides the designers with a library of configurable TLM components.	**1**
Eindhoven University of Technology	Sander Stuijk	SDF3	The SDF3 tool implements a state-of-the art design flow that can map a throughput-constrained application modeled with a Synchronous Dataflow Graph onto a NoC-based MP-SoC while providing timing guarantees. The design flow analyzes the resources requirements of the application, allocates the required resources in the NoC-based MP-SoC, and schedules accesses to shared resources. At every step of the flow, the complete state of the design flow can be outputted in XML.	**2**

Université de Bretagne Sud	Rachid Dafali	µSPIDER CAD TOOL: CASE STUDY OF NOC IP GENERATION FOR FPGA	This demo presents the µSpider CAD tool for network on chip design under latency and bandwidth constraints and described the different steps of the associated design flow. We show: 1) how the tool can be used to automatically generate a NoC IP compliant with Xilinx EDK tool and 2) a real case implementation of a video application running on a Virtex2pro FPGA, the architecture includes 2 Mblaze, 1 PPC and our NoC IP.	**3**
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University of Bonn	Andreas Raabe	A Reconfiguration Simulation Library For SystemC	This demonstration presents a library for modelling reconfiguration in SystemC combining IP reuse and high-level modelling with reconfiguration. Control statements and techniques that allow safe process controlling in conjunction with SystemC language constructs are presented. A case study proves its applicability.	**6**
Chemnitz University of Technology	Uwe Proß	Specification data gathering	The Software gathers information about the system and its behavior on specification level and will check this specification for consistency. It enables Reuse of testcases as well as requirements and cost engineering. Code export to several tools and languages integrates SpecScribe in the design flow.	**7**
Universität Karlsruhe	Jürgen Becker	MORPHEUS integrated toolset	The toolset compiles annotated c-code to ARM binaries while replacing the annotated function calls with calls the equivalent configurations on one of the heterogeneous reconfigurable engines of the MORPHEUS SoC. Additionally the toolset synthesizes the necessary control codes for the NoC to feed data to the engines.	**8**
16:00 - 18:00	**Session**	**Hardware Solutions**		**UB 2.4**
Université de Bretagne Sud	Pierre Bomel	A mixed (hardware and software) rapid prototyping platform.	PALMYRE is set of hardware components and software tools enabling the rapid prototyping of telecom-oriented application. DSPs from Texas Instruments and FPGAs from Xilinx can be freely mixed to build a specific computing and communication topology. The demonstration is a pipeline of two DSPs and an FPGA Viterbi decoder. Thanks to the GALS/LIS approach the system is data regulated and can be stopped and restarted without loss of any data or synchronization between DSPs and FPGA.	**1**

Université de Bretagne Sud	Pierre Bomel	A lightweight and remote partially reconfigurable platform	We present the concept of a networked lightweight and partially reconfigurable platform assisted by a remote bitstreams server. We propose a software and hardware architecture as well as a new data-link level network protocol implementation dedicated to dynamic and partial reconfiguration of FPGAs. These systems target embedded applications with very scarce hardware resources taking advantage of dynamic, specific and optimized architectures.	**2**
Universidad Complutense de Madrid	Francisco Vallejos	OS based Wireless Body Area Network for ECG	We present a complete architecture of a Wireless Body Area Network for ECG (electrocardiogram) monitoring.The network is composed of five nodes and a base station. The nodes proccess the ECG signal that they senseand they send information to the base station when a special event occurs, depending on the application. Wehave developed a new TDMA protocol that reduces the energy consumption associated with the radio.	**3**
Université de Bretagne Sud	Philippe Coussy	GAUT – A High-Level Synthesis tool for DSP applications	Starting from a pure C function GAUT generates a potentially pipelined architecture composed of a processing unit, a memory unit, a communication unit with a GALS/LIS interface. The synthesis constraints are the data average throughput, the clock frequency, the FPGA/ASIC target technology and optionally the memory architecture/mapping, the I/O timing diagram. GAUT generates an IEEE-P1076 VHDL file and test benches which is an input for commercial logical synthesis tools like ISE/Foundation from Xilinx, Quartus from Altera or DC from Synopsys.	**4**
Eindhoven University of Technology	Andreas Hansson	CoMPSoC - A Composable and Predictable Multi-Processor System-on-Chip Template	We propose a Composable and Predictable Multi-Processor System-on-Chip (CoMPSoC) platform and mapping methodology. Multiple real-time jobs can run simultaneously. Incremental integration and platform virtualisation are supported. The real-time jobs are analysed and verified independent of one another, using state-of-the-art dataflow techniques.	**5**
University of Bonn	Stefan Hochgürtel	A broadband FFT-Spectrometer at work	We present a fully functional FFT-spectrometer card, calculating 2048 channels at a bandwidth of up to 1500 Mhz. Multiple parameters as well as the complete spectrometer-core can be altered at run-time over ethernet. Spectra, which are also send to a PC by ethernet, will be presented interactively.	**6**
Technical University of Denmark	Jan Madsen	Formal Verification of Design Properties of Hardware Architectures	We present a formal language for hardware models based on the Gezel hardware description language developed and maintained by Virginia Tech, USA. We show how the language can be used in connection with verification by relating the semantical domain to timed-automata using the UPPAAL system. We will also demonstarte a formal verification of design properties of a few simple example circuits including the Simplified Data Encryption Standard (SDES) Algorithm and different algorithmic implementations of the Greatest Coomon Divisor.	**7**

University of Rostock	Peter Danielis	Trust-by-Wire in Packet-switched IP Networks: Calling Line Identification Presentation for IP	The packet processing system IPclip (IP Calling Line Identification Presentation) is presented. It is implemented on an FPGA board and configurable at runtime via a graphical configuration tool. The functionality is demonstrated in a localization scenario using an analysis tool and Google Earth.	**8**

Thursday, March 13, 2008

10:00 - 12:00	**Session**	**System Exploration with Software and Hardware**		**UB 3.1**
Eindhoven University of Technology	Sander Stuijk	SDF3	The SDF3 tool implements a state-of-the art design flow that can map a throughput-constrained application modeled with a Synchronous Dataflow Graph onto a NoC-based MP-SoC while providing timing guarantees. The design flow analyzes the resources requirements of the application, allocates the required resources in the NoC-based MP-SoC, and schedules accesses to shared resources. At every step of the flow, the complete state of the design flow can be outputted in XML.	**1**
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University of Paderborn	Christopher Pohl	Hardware-in-the-Loop Simulations with Matlab/Simulink/ModelSim for FPGA based designflows	This demonstrator shows the design flow and a working example of our Hardware-in-the-Loop Design Environment for FPGAs. Arbitrary VHDL designs can be automatically integrated into simulation or visualization tools, enabling functional verification and real time monitoring of that hardware design.	**4**
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Politecnico di Milano	Vittorio Zaccaria	System Tuning Shell: A Design Space Exploration Tool	System Tuning Shell is a design space exploration tool for supporting platform-based design. The tool is a flexible and modular system optimizer that allows users to plug-in custom system models and apply several optimization strategies to derive trade-offs on the system cost functions.	**6**

TU München	Christopher Claus	Hardware/software architecture of an algorithm for vision-based real-time vehicle detection in dark environments	The demonstrator runs on an ML310 board from Xilinx. Images are loaded from the connected hard drive into the main memory (DDR SDRAM) which is located on the board. From there, the pixel data can be accessed by a hardware coprocessor called TaillightEngine which is able to detect cars in dark environments. The processed pixels are written back into the main memory from where they can be accessed and be displayed on an external monitor.	**7**
12:00 - 14:00	**Session**	**High Level Synthesis**		**UB 3.2**
University of Tehran	Mahshid Sedghi	TLM Synthesis Studio	TLM Synthesis Studio is an environment to help system level designers start the design and implementation of their systems from transaction level. It supports OSCI TLM library and SystemC. It also provides the designers with a library of configurable TLM components.	**1**
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Norwegian University of Science and Technology	Saeeid Tahmasbi Oskuii	Low Power Partial-Product Reduction-Tree Generator for Parallel Multipliers	In this demonstration, a method will be presented for generation of power-efficient parallel multipliers in such a way that its partial products are connected to minimize activity. At each stage of the reduction tree, a simulated annealing optimizer uses power cost numbers from a specially implemented probabilistic gate-level power estimator and selects a power-efficient solution.	**6**
University of Tehran	Parisa Razaghi	A Platform for Multi-Language Mixed-Signal Simulation	Mixed-Signal Simulator is a mixed-signal, mixed-domain, and mixed-language design environment which supports VHDL-AMS 1999, VHDL-2002, Verilog 2001, SystemVerilog 2005 assertions, and SystemC 2005.	**7**
14:00 - 16:00	**Session**	**Physical Design, Modelling and Exploration**		**UB 3.3**
Université de Bretagne Sud	Pierre Bomel	A mixed (hardware and software) rapid prototyping platform.	PALMYRE is set of hardware components and software tools enabling the rapid prototyping of telecom-oriented application. DSPs from Texas Instruments and FPGAs from Xilinx can be freely mixed to build a specific computing and communication topology. The demonstration is a pipeline of two DSPs and an FPGA Viterbi decoder. Thanks to the GALS/LIS approach the system is data regulated and can be stopped and restarted without loss of any data or synchronization between DSPs and FPGA.	**1**
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Technical University of Braunschweig	Steffen Stein	Advances in Symbolic Performance Analysis	We will demonstrate the latest advances in formal performance analysis and its application for runtime performance control. We will demonstrate approaches to embedded performance control, current research in event stream modeling and analysis approaches applicable for MPSoC.	**4**

University of Tehran	Homa Alemzadeh	SystemC Studio: Translation for TLM Combined Simulation and Synthesis	SystemC Studio provides an interface between RT level VHDL/Verilog descriptions and high level descriptions in SystemC and SystemC TLM. This is done by translating VHDL/Verilog codes into RT level SystemC, linking them with post-synthesis SystemC codes coming from synthesis of high level TLM descriptions, and generating a SystemC/C++ model of the entire hardware to be simulated and verified. This environment also provides SystemC translation to VHDL for RTL synthesis of post high-level synthesis TLM descriptions.	**5**