Extending the RISC-V LLVM backend to Support Fault-tolerant Computing

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Abstract

Fault tolerance against random hardware errors can be reached by software redundancy methods, which is also known as software-implemented hardware fault tolerance (SIHFT). As compiler optimization can remove this redundancy, SIHFT methods need to be implemented in the compiler backend. In this talk we present an extension of the RISC-V 32bit and 64bit LLVM backend that implements a wide range of SIHFT methods, namely EDDI, SWIFT, nZDC, CFCSS, RASM and a new method developed by us known as REPAIR. These methods conduct either instruction duplication (data flow hardening) or signature monitoring (control flow hardening). The backend also supports selective hardening of critical functions to generate resilient RISCV binaries. It is planned to release the project as open source in the near future.

Biography

 M.Sc. Uzair Sharif is currently pursuing his PhD studies at TU Munich, Germany. The focus of his dissertation is to design efficient fault tolerant methods geared towards safety-critical embedded systems. His research interests mainly encompass major topics of electronics engineering such as computing, HW/SW co-design, statistical signal-processing etc.