Eingeladener Vortrag: 3D Design Space asks for a new Product Development Process

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Kurzfassung

Many market places for micro-electronics products ask for aggressive "More than Moore" integration densities and complexities. Driver was the mobile communication market (every competitive smart phone holds 3D chip stacks).Today, the drivers are also the roadmaps for e.g. automotive, multimedia, computing, energy efficiency and security application requirements. Different 3D integration technologies are popping up just now: starting from side by side System in Package (SiP) we observe "chip stacks" using TSV and TEV concepts (thru silicon and encapsulation via). Also various "embedding" technologies get accepted both in silicon and pcb carrier and interposer concepts. So, 3D technologies are emerging rapidly. Looking on the design methodology and tool scenario: The priority on 3D is pointed out and point tools exist, so we do not have very efficient solutions but we can execute complex 3D product designs (manual work – adequate design automation will come). So we have technologies and design methodologies not fully in place but on the horizon.

Still there is a big question mark: why are the 3D concepts not really generating a revolution in the market places. Feature and performance benefits are obvious. My answer is: because we do not have a well established product development process which enables the comparison of the competitiveness of 3D product integration concepts in relation to well known 2D solutions. This process has to take into account all significant competitiveness criteria like: Cost of Sales, NRE Cost and Time to Market, Technology and Design Risks (Yield), Testing, Software oriented capabilities, DfM, DfT, EMI. Today we execute all those evaluations – but we do it at the end of the development process – as a sign off. What we need is the capability to run those comparisons in the early concept phase and here we need new methodologies and tools – and a changed engineering mindset.

Curriculum Vitae

Jochen Reisinger is a Director with Infineon's central Methodology Team (Chip-Package-Board Co-Design) – working at Design Center Villach (A) and Munich. After his studies on Telecommunications & Electronics at Technical University in Graz, JR did join Siemens Semi Group in Munich. He set up a MOS-Analog Design Team in Villach to develop the first signal processing codec-filter. Back to Munich in 1993 Testing and Product Engineering became the main focus. JR is heading the CATRENE EU-project CoSiP and supports 3D collaboration projects.