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## Verisity, Inc.

# Company Presentation: Verisity Design, Inc.



### "Improving Shareholder Value by Separating Verification from Design"

The semiconductor industry continues to strive to manage the ever increasing risk of leaving a corner case bug that becomes the next front page story for EETimes. With cost of failure fast becoming a common agenda point in many semiconductor board room meetings around the world, how can you deliver to the ever growing demands of increasing shareholder value?

Managing scarce resources to deliver sustainable competitive advantage is the platform upon which most of today's strategic thinking is built. Yet in the complex world of semiconductor product design we continue to see the promotion of the „jack of all trades“ designer in the false belief that it actually reduces costs.

Separating verification from design is a natural evolution to the necessary specialization that has become functional verification today. Why do accounting regulations demand that you employ armies of auditors to review your end of year accounts? When, not so many years ago, you could get away with your own accountants completing this function.

Auditors are much the same as verification engineers. They are approaching the problem from a completely different perspective. They do not come with the cognitive incompetence of „I know that's right, because I produced it!“ The global company graveyard is littered with the tomb-stones of many household names that have made this mistake, Enron included.

In this presentation, Verisity will deliver a solution to provide unique value that can be generated when you separate the concerns of functional verification from design. Reducing the cost of failure risks and significantly improving the effectiveness of your scarce engineering resource by automating the process of verification itself.

### Presenter

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