Economics of IP

Business Session 1

Measure or Die - Design Productivity Keynote

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Abstract

Ever shrinking silicon geometries and the resulting growing number of transistors that can be implemented on a single die will continue to fuel the trend towards systems on a chip (SoCs). For the same reasons that growing complexity led to the adoption of standards in the world of electronic systems. Standards are also finding their way into SoCs. As a result, an increasing portion of these SoCs can be assembled from pre-designed blocks that implement functionality defined by standards.

This has created a business opportunity for so called IP vendors to develop 'ready to use' standards-based IP blocks and market them to semiconductor companies who integrate these IP blocks into SoCs. The underlying assumption is that it should be economically more efficient to have a small number of IP vendors develop these IP blocks for the entire industry than each semiconductor company developing them for their own use.

From an IP vendor point of view the fundamental question is how large is the market for a particular new standard. In other words, how many SoCs will need an IP block that implements that standard. This question needs to be answered well before semiconductor companies start sourcing IP blocks for that standard, and many times in light of various new standards competing for the same role. Waiting to see how the market acceptance of these new standards develops is hardly an option. Whoever is first to market with a high quality IP block usually ends up dominating the market.

From the point of view of an IP user, the question is how much of the total cost of developing, verifying, and integrating a particular standards-based function can be saved by procuring it as an IP block, be it from some other department in the same company or from an external IP vendor. Assuming the IP component fits architecturally into the SoC, invariable the all decisive factor is the quality of the IP block. If an externally procured IP component requires, for lack of quality or confidence, to undertake a complete verification effort, much of the expected cost advantage will be lost.

This talk will examine the economics underlying standards-based IP from the perspective of both the IP vendor and that of the user of IP.

Curriculum Vitae

 Joachim Kunkel is the Vice President of Engineering and Design Solutions at Synopsys, Inc. Prior to joining Synopsys Joachim was a managing director of CADIS GmbH, a company he had co-founded in 1989 in Aachen, Germany. CADIS GmbH focused on the development of system level design tools for digital signal processing and

providing specialized design services for wireless communication systems.

From 1984 to 1989 Joachim was a research assistant at the Aachen University of Technology's "Lehrstuhl fuer Elektrische Regelungstechnik", where he conducted research in the area of system level simulation techniques for digital signal processing, with special emphasis on parallel computing.

Joachim Kunkel received a "Dipl.-Ing. der Nachrichtentechnik" degree (MSEE equivalent) from the Aachen University of Technology, Aachen, Germany in 1984.