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# The CELL Microprocessor

## edaForum05 Presentation

### Business Session I

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### The CELL Microprocessor

#### Abstract

CELL is the result of a deep partnership between SCEI/Sony, Toshiba, and IBM. The processor is optimized for compute-intensive and broadband rich media applications. Correct operation was observed in the lab on 1st-pass hardware at frequencies well over 4GHz, supporting a peak performance of over 256Gflops. On well behaved applications (graphics, media, DSP), the chip has demonstrated a 10x to 100x advantage in performance/ chip and performance/Watt.

Such a challenging design required new design concepts and design styles, which will be addressed in our presentation. We will also give an overview of the CELL processor and the major design challenges.

Early details of Cell s technical specifications were disclosed in papers delivered at San Francisco s International Solid State Circuit Conference (ISSCC) in February, 2005. The documents released in August, 2005 broaden the disclosures and put the details into the framework of the Cell Broadband Engine Architecture.

By opening up a wide set of technical specifications to software developers, business partners, academic and research organizations, and potential customers, IBM, Sony and Toshiba continue their diligent efforts to stimulate the creation of Cell-based applications. The goal: establish a thriving community of interest and innovation around Cell, allowing all interested parties to rapidly evaluate and utilize Cell technology.

#### Biography



**STSM, Microprocessor Development**

#### IBM Böblingen

**She joined IBM in 1999. She is an expert in the field of Floating-Point unit (FPU) design and high frequency microprocessor design. She belongs to the CELL- Design-Team right from the**

**beginning,**

**leading the design work for the FPUs of the CELL processor. She is now leading a second global team, designing high-performance FPUs for future eServers. Prior to joining IBM, she was a professor (Privatdozent) for computer science at the University of Saarland. She is still lecturing on different topics of computer architecture. She holds a Ph.D. in Computer Science and an M.Sc. in Mathematics.**

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