The Answer is Formal Verification - What was the Question?

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Abstract

Listening to some industry experts, the bar for formal verification has been raised to the point where success is measured by the time that it takes for formal methods to replace the more traditional simulation based verification. This is not a helpful stance for the industry or academia. Formal methods are a good complement, but not a replacement technology, whose adoption will be tempered by both technical and economic considerations. Instead of pushing the mathematical basis of a tool, we must concentrate on such issues as: how does it increase an engineer's productivity? How will it reduce the overall verification time and expense? And how will it ensure that the important bugs have been eradicated? In this presentation both the economic and technical aspects will be explored with one possible outcome being presented.

Curriculum Vitae

 Brian Bailey is the chief technologist for the Design Verification and Test Division of Mentor Graphics. In this role, Bailey is responsible for setting the technology direction for the group. Previously, Bailey was involved in the creation of the Mentor Graphics Seamless Co-Verification Environment for hardware and software co-simulation. Prior to his work with the Seamless product, Bailey worked with a variety of simulation technologies, including simulation acceleration, emulation, mixed-signal and multi-level simulators. Bailey began his career in the aircraft design business before leaving to work on the emergence of RTL simulation. Bailey graduated from Brunel University in England in 1981 with first class honors in Electrical and Electronic Engineering. He is the Chair of the Accellera Interfaces technical committee and has been active in a number of other standards bodies. He has two patents issued and a number of others pending.