Imec and Atrenta develop exploration flows for 3D ICs

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Atrenta and imec's 3D integration IIAP (industrial affiliation program) have jointly developed an advanced planning and partitioning design flow for heterogeneous 3D stacked ICs. A flow allowing robust, accurate partitioning and prototyping early in the design process is critical to make cost-effective 3D systems and to get them to market fast.

The flow under development allows minimizing the number of design iterations, facilitating a cost- and time-effective search of the solution space. To design innovative applications with 3D stacked dies, the ability to do early planning and partitioning is critical. The number of potential solutions for any given system design problem (e.g., front to front, front to back, silicon interposer, technology choice for slices, via configurations, partitioning, etc.) is very large. Exploring this solution space through multiple full designs is simply too expensive and time-consuming. This makes it critically important to perform robust, accurate partitioning and prototyping early in the design process, well before detailed implementation begins.

There are other significant challenges for 3D design, such as the thermal profiles (heat dissipation) and the mechanical stress caused by assembly configurations. Imec has developed compact thermal and mechanical models for rapid generation of heat dissipation and mechanical stress maps and has validated them using real 3D DRAM-on-logic packaged devices. When combining the design floor plans produced by Atrenta's SpyGlass Physical 3D prototyping tool with the stress models developed by imec, different scenarios can be assessed quickly and the best option can be chosen in advance of a full design implementation.

Visit imec at [www.imec.be](http://www.imec.be)

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