Goals

The primary project goal of VeronA is the development of fundamental elements of an integrated verification methodology for integrated analog circuits. Thereby, emphasis is laid on the suitability of the developed methods for industrial application.

VeronA targets a considerable commercial benefit through an intense improvement of the design correctness, so that the verification effort – in spite of increasing circuit complexity – at least remains constant in the future. For this purpose, the efficiency of the verification process itself will be increased by 30 % at least. At the same time, the number of redesigns will be reduced by 20 %. Thus, the improved verification methods developed within this project will counteract the widening of the "design gap".

The project results, such as rules for the verification-oriented modeling, methods for mixed-signal/mixed-level simulation and formalized procedures are expected to become key elements for the efficient verification of analog circuit blocks. They will essentially improve the present situation of verification in terms of efficiency and quality. At least, this ultimately will lead to qualitatively higher valued and more reliable electronic products.

Verification checks whether a circuit or system conforms to a specification or model.

The following technical goals are in the focus of the project:

- Development of methods and rules for the creation of models which are suitable for verification in different levels of abstraction, because they can be simulated quickly and also sufficiently describe many physical effects (e.g. mixed-discipline or temperature).
- Investigation and development of formal verification methods for analog circuits, namely model checking and equivalence checking.
- Development of methods for assertion-based verification, as well as of formal procedures for performance and tolerance verification.
- Implementation of an integrated methodology for multi-level verification of analog systems considering mixed-signal/mixed-domain aspects and using the aforementioned points.

Partners

ATMEL

BOSCH

cadence

Infineon

MunEDA

qimonda

Subcontractors

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VeronA

Verification of Analog Circuits

a public funded EDA research project

Runtime: 06/2006 - 05/2009

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Abstract

The VeronA project creates a basis for an automated verification of analog circuits and systems. Its goal is to develop fundamental elements of an integrated verification methodology for integrated analog circuits, such that the analog parts of mixed-signal chips can be verified along with the digital part. Therefore, new methods and tools are developed which exploit formalized verification and target verification-oriented modeling.

Ekompass

Bundesministerium für Bildung und Forschung

The VeronA project (FKZ: 01 M 3079) is supported in accordance with the BMBF "Nanoelectronics" sponsorship scheme within the scope of the Ekompass sponsorship complex of the Federal Ministry of Education and Research (BMBF).

WP1: Verification oriented modeling

WP1.1: Simulation performance
(ATM, CDN, RB, IFX)
WP1.2: Verification-oriented modeling for very high temperatures
(IFX)

The verification of analog circuits and systems is based almost exclusively on circuit simulation, whereby the analog functions must be described through behavioral models for mastering the complexity of today's systems. The simulation time mainly depends on the performance of the behavioral models. Behavioral models that can be simulated quickly (with an accuracy that is sufficient for the application) must be developed to reach the goal of a highly efficient verification of a complete A/MS IC.

One challenge is the efficient formulation of these models. This includes an investigation of different modeling approaches (e.g. equation-based, black-box) and of the simulation algorithms used. It is the goal of the work to reduce the simulation time through improved behavioral models by at least a factor of 100 compared to transistor-level simulation.

The other big challenge is the accuracy needed for these models. Here one crucial aspect, especially for the automotive industry, is the electro-thermal behavior at very high temperatures (300°C and above). If this is not described correctly, especially for power transistors, severe verification errors can not be excluded.

Structure of VeronA

VeronA comprises three work packages (WP) named
WP1: "Verification oriented modeling"
WP2: "Formalized verification"
WP3: "Multi level verification"

which are divided into several tasks, shown on this page. While WP1 and WP2 deal with fundamental verification elements like modeling and formalization, WP3 is focused on strategies for multi-level verification.

Structure

WP2: Formalized verification

WP2.1: Methods for Model Checking
(CDN, RB)
WP2.2: Methods for Equivalence Checking
(RB, QAG)
WP2.3: Simulation-based methods
(CDN, RB, IFX, QAG, MUN)

Formal verification methods such as model checking and equivalence checking are already used for the verification of digital circuits. With the research of formal verification methods for analog circuits, the project partners are breaking new ground scientifically. This step is necessary to enable a complete verification of analog circuits.

In addition, assertion-based verification – previously applied exclusively to digital circuits – is to be transferred to the analog domain in VeronA. The goal is to check compliance with conditions (assertions) during the simulation just as in the digital domain, which dramatically simplifies recognition and localization of errors. The challenge consists in formulating the essentially more complex conditions and to review them with the aid of a circuit simulator, without increasing the simulation time appreciably in the process.

WP3: Multi level verification

WP3.1: Application-oriented verification of complete automotive ICs
(ATM, RB)
WP3.2: System-level co-simulation with analog components
(ATM, CDN, RB)
WP3.3: Application of models across abstraction levels
(ATM, MUN)

The existence of modern simulation tools, description languages, and formalized methods is not sufficient for the manifold tasks necessary for verification of complete A/MS-ICs, which is still a big design challenge. Thereby, especially strategies and methods for efficient verification of analog parts and its interfaces are lacking. Here the work in WP3 puts on.

Ultimately, approaches and methods are researched that enable an application-oriented multi-level verification of analog components. This work package will combine results from the modeling area and from the work on formal methods to form new overall approaches. Their efficiency will be demonstrated using examples from the automotive and mobile communications area.

With respect to the opportunity to enhance the almost simulation based verification of special applications, the use of coupled simulators is considered, especially concerning their interfaces. Therefore, co-simulation solutions are investigated with respect to the connection of analog parts within system simulations.

Another aspect of WP3 concerns the difficult task to explore methods to consider process and operational tolerances on different abstraction levels.

Enhanced formalization will raise coverage – and thus quality – of the verification and will relieve circuit designers. Additionally, systematic design space exploration will be ensured by considering process and operational tolerances.